Department of Electronics and Communication Engineering

M.Tech. VLSI
Curriculum and Syllabus

(Applicable to the students admitted during AY: 2022-23)

School of Engineering and Sciences
SRM University *AP*, Andhra Pradesh

Department Vision

To be a globally recognized leader in the field of Electronics and Communications, by fostering innovation through cutting-edge collaborative research to inform interdisciplinary education.

Department Mission

1. Create inclusive and highly motivated individuals and leaders who promote diversity, innovation, creativity, and a high sense of responsibility towards societal progress.
2. Strive for excellence by promoting interdisciplinary education and research through global collaborations.
3. Deliver state-of-the-art research-based education that equips students with the skills to address contemporary challenges and contribute to the field's advancement.
4. Foster a culture of innovation and entrepreneurship, by working closely with leading industry partners to translate ideas into real-life solutions.
5. Aim to be a global knowledge hub by collaborating with leading institutions and industries.

Program Educational Objectives (PEO)

1. Enable the postgraduate students to learn the fundamentals of VVLSI deeply and lay a strong foundation for their professional careers or higher studies.
2. Train the students to have hands-on VLSI System design skills which can be applied to solve industrial and research problems in an interdisciplinary environment.
3. Train the students to have comprehensive knowledge and skills in VLSI technologies which can be applied to the given problems in industrial and research multi-disciplinary environments.
4. Facilitate the development of effective communication skills, lifelong learning, leadership qualities and ethical professional conduct across their higher education and career paths.

Mission of the Department to Program Educational Objectives (PEO) Mapping

	PEO 1	PEO 2	PEO 3	PEO 4
Mission Statement 1	3	3	2	2
Mission Statement 2	3	3	2	2
Mission Statement 3	3	2	3	2
Mission Statement 4	3	2	3	3
Mission Statement 5	3	3	3	2

Program Specific Outcomes (PSO)

1. Recognize, research, and resolve a wide range of practical issues in the field of VLSI.
2. Develop skills to build and create systems in the expanding fields of VLSI to solve the problems of the modern economy.
3. Demonstrate exemplary leadership attributes and actively pursue the advancement of many entities, including organizations, the environment, and society at large. by upholding their professional obligations with a strong commitment to ethical conduct.

Mapping Program Educational Objectives (PEO) to Program Learning Outcomes (PLO)

Program Learning Outcomes (PLO)													
PEOs	POs										PSOs		
	Engineering Knowledge	Design Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Lifelong Learning	PSO 1	PSO 2	PSO 3
PEO 1	3	3	3	3	2	1	3	2	2	2	3	2	2
PEO 2	3	3	3	3	3	1	3	1	2	2	3	2	3
PEO 3	3	3	3	3	3	3	3	3	3	3	2	3	3
PEO 4	2	3	2	2	2	3	3	1	2	2	3	3	3

Category Wise Credit Distribution			
Course Sub-Category	**Sub-Category Credits**	**Category Credits**	**Learning Hours**
Ability Enhancement Courses (AEC)		0	0
University AEC	0		
School AEC	0		
Value Added Courses (VAC)		0	0
University VAC	0		
School VAC	0		
Skill Enhancement Courses (SEC)		0	0
School SEC	0		
Department SEC	0		
SEC Elective	0		
Foundation / Interdisciplinary courses (FIC)		0	0
School FIC	0		
Department FIC	0		
Core + Core Elective including Specialization (CC)		34	1020
Core	25		
Core Elective (Inc Specialization)	9		
Minor (MC) + Open Elective (OE)	6	6	180
Research / Design / Internship/ Project (RDIP)		32	960
Internship / Design Project / Startup / NGO	0		
Internship / Research / Thesis	32		
Total		**72**	**2160**

Semester wise Course Credit Distribution Under Various Categories						
Category	**Semester**					
	I	**II**	**III**	**IV**	**Total**	**%**
Ability Enhancement Courses - AEC	1	0	0	0	0	**0**
Value Added Courses - VAC	0	0	0	0	0	**0**
Skill Enhancement Courses - SEC	0	0	0	0	0	**0**
Foundation / Interdisciplinary Courses - FIC	0	0	0	0	0	**0**
CC / SE / CE / TE / DE / HSS	16	17	0	0	34	**47**
Minor / Open Elective - OE	3	0	3	0	6	**8**
(Research / Design / Industrial Practice / Project / Thesis / Internship) - RDIP	1	4	12	15	32	**44**
Grand Total	**21**	**21**	**15**	**15**	**72**	**100**

Note: L-T/D-P/Pr and the class allocation is as follows.

a) Learning Hours : 30 learning hours are equal to 1 credit.

b) Lecture/Tutorial : 15 contact hours (60 minutes each) per semester are equal to 1 credit.

c) Discussion : 30 contact hours (60 minutes each) per semester are equal to 1 credit.

d) Practical : 30 contact hours (60 minutes each) per semester are equal to 1 credit.

e) Project : 30 project hours (60 minutes each) per semester are equal to 1 credit.

SEMESTER - I								
S. No	**Category**	**Sub-Category**	**Course Code**	**Course Title**	**L**	**T/D**	**P/Pr**	**C**
1	Core	CC	VLS 511	CMOS Digital IC Design	3	0	0	3
2	Core	CC	VLS 511L	CMOS Digital IC Design Lab	0	0	1	1
3	Core	CC	VLS 512	Embedded Programming	3	0	0	3
4	Core	CC	VLS 512L	Embedded Programming Lab	0	0	1	1
5	Core	CC	VLS 513	VLSI Technology	3	0	0	3
6	Core	CC	AML 501	Machine Learning Techniques	3	0	0	3
7	Core	CC	AML 501L	Machine Learning Techniques Lab	0	0	3	2
8	Elective	OE		Open Elective / Minor	3	0	0	3
9	AEC	AEC	EGL 501	English for Research Paper Writing	1	0	0	1
10	RDIP	RDIP	VLS 548	Fundamentals in Business, Innovation and Project Management	1	0	0	1
				Semester Total	**17**	**0**	**5**	**21**

SEMESTER - II								
S. No	**Category**	**Sub-Category**	**Course Code**	**Course Title**	**L**	**T/D**	**P/Pr**	**C**
1	Core	CC	VLS 521	VLSI Testing and Verification	3	0	0	3
2	Core	CC	VLS 521L	VLSI Testing and Verification Lab	0	0	2	1
3	Core	CC	VLS 522	CMOS Analog and Mixed Signal IC Design	3	0	0	3
4	Core	CC	VLS 522L	CMOS Analog and Mixed Signal IC Design Lab	0	0	1	1
5	TE	TE	TE	Technical Elective - I	3	0	0	3
6	TE	TE	TE	Technical Elective - II	3	0	0	3
7	TE	TE	TE	Technical Elective - III	3	0	0	3
8	RDIP	RDIP	VLS 526	Mini Project I	0	0	2	2
9	RDIP	RDIP	RM 101	Research Methodology for IPR	2	0	0	2
				Semester Total	**17**	**0**	**8**	**21**

SEMESTER - III								
S. No	**Category**	**Sub-Category**	**Course Code**	**Course Title**	**L**	**T/D**	**P/Pr**	**C**
1	Elective	OE		Open Elective / Minor	3	0	0	3
2	RDIP	RDIP	VLS 539	Project Part - I	0	0	12	12
				Semester Total	**3**	**0**	**12**	**15**

SEMESTER - IV								
S. No	**Category**	**Sub-Category**	**Course Code**	**Course Title**	**L**	**T/D**	**P/Pr**	**C**
1	RDIP	RDIP	VLS 549	Dissertation Project Final	0	0	15	15
				Semester Total	**0**	**0**	**15**	**15**

List of Technical Elective								
S. No	**Category**	**Sub-Category**	**Course Code**	**Course Title**	**L**	**T/D**	**P/Pr**	**C**
1	TE	TE	VLS 533	Semiconductor Device Modelling	3	1	0	4
2	TE	TE	VLS 535	Hardware Accelerators for IoT Edge Computing	3	0	1	4
3	TE	TE	VLS 562	Sensor Technology and MEMS	3	1	0	4
4	TE	TE	VLS 530	CAD for VLSI	3	0	1	4
5	TE	TE	VLS 555	More than Moore’s electronics	3	1	0	4

SRM University *AP*, Andhra Pradesh
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CMOS Digital IC Design

Course Code	VLS 511	**Course Category**	Core Course	**L**	**T**	**P**	**C**
				3	0	0	3
Pre-Requisite Course(s)		**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	ECE	**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. To understand the fundamental principles of CMOS technology, including the operation of MOS transistors, logic gates, and basic building blocks.
2. To learn the techniques for designing and analyzing CMOS digital circuits, including combinational and sequential logic circuits.
3. To gain proficiency in creating layout designs for CMOS circuits (considering area, power, and performance) and understand the importance of timing in digital circuits, and learn how to perform timing analysis for CMOS circuits.
4. To apply the knowledge gained in the course through hands-on projects that involve the design, simulation, and layout of CMOS digital circuits.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Understand the fundamental principles of CMOS Technology along with its advantages and limitations	2	85%	80%
Outcome 2	Design both combinational & sequential circuits using CMOS technology	3	80%	75%
Outcome 3	Create layout designs for CMOS digital circuits and understand the impact of the fabrication process on circuit design	3	85%	70%
Outcome 4	Apply theoretical knowledge to real-world digital IC design projects	3	80%	70%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	2	2	2	3	2	2	2	3	2	2	3	2
Outcome 2	3	3	3	2	1	2	2	3	3	3	2	3	3
Outcome 3	3	3	3	2	1	2	2	3	2	3	2	3	3
Outcome 4	3	3	3	2	3	3	3	3	3	3	3	3	3
Average	3	3	3	2	2	2	2	3	3	3	2	3	3

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References
Unit 1	**MOSFET Introduction and Layout of CMOS Logic Circuits**	**9**		
	Basic MOSFET Characteristics– Threshold Voltage, Body Bias concept, Current- Voltage Characteristics – Square-Law Model	2	1	1,2
	MOSFET Modeling– Drain-Source Resistance, MOSFET Capacitances	1	1	1,2
	Geometric Scaling Theory– Full-Voltage Scaling, Constant-Voltage Scaling, Challenges of MOSFET Scaling	2	1	1,2
	CMOS fabrication processing steps	1	1	1,2,4,6
	Design Rules, Stick diagram, Layout of logic circuits	2	1,3	
	Layout of logic circuits, latch-up	1	1,3	1,2,4,6
Unit 2	**Switching Properties of MOSFET and CMOS Inverter**	**8**		
	Static and dynamic characteristics of Pass Transistors	1	1,2	1,2
	Transmission Gate, TG based logic circuits, Introduction to CMOS Inverter	2	1,2	1,2
	CMOS Inverter - DC Characteristics, Noise Margins, Layout Considerations	1	1,2	1,2
	Inverter Switching Characteristics, Transient Effects on the VTC, RC Delay Modeling, Elmore Delay, Output Capacitance	2	1,2	1,2
	Inverter Design – DC Design, Transient Design, Driving Large Capacitive Loads	2	1,2	1,2
Unit 3	**Static CMOS Logic Elements & Power Dissipation in CMOS Logic Circuits**	**9**		
	CMOS NAND Gate, CMOS NOR Gate	1	2,3	1,2,3
	CMOS AND, OR, NOT, and Complex Logic Functions	2	2,3	1,2,3
	CMOS SRAM and DRAM Cell	1	2,3	1,2,3
	Dynamic Power Dissipation– Switching Power Dissipation	2	2,3	1,2,3
	Short Circuit Power Dissipation, Glitching Power Dissipation	1	1,3	1,2,3
	Static Power Dissipation, Diode Leakage Current, Subthreshold Leakage Current	2	1,3	1,2,3
Unit 4	**Dynamic Logic Circuit Concepts and CMOS Dynamic Logic Families**	**9**		
	Charge Leakage in CMOS circuits	2	2,4	1,2,5
	Charge Sharing, Dynamic RAM Cell	2	2,4	1,2,5
	Clocked-CMOS	2	2,4	1,2,5
	Pre-Charge/ Evaluate Logic, Domino Logic	2	2,4	1,2,5
	CMOS Single-Phase Logic	1	2,4	1,2,5
Unit 5	**Issues In Chip Design**	**8**		
	ESD Protection	2	2,3,4	1,2,5
	On-Chip Interconnects – Line Parasitics	1	2,3,4	1,2,5
	Modeling of the Interconnect Line	2	2,3,4	1,2,5
	Clock Distribution	2	2,3,4	1,2,5
	Input-Output circuits	1	2,3,4	1,2,5
	Total	**43**		

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)				End Semester Exam (50%)
		CLA-1 (10%)	Mid-1 (15%)	CLA-2 (15%)	CLA-3 (10%)	
Level 1	Remember	40%	60%		50%	30%
	Understand					
Level 2	Apply	60%	40%	20%	50%	60%
	Analyse					
Level 3	Evaluate			80%		10%
	Create					
Total		**100%**	**100%**	**100%**	**100%**	**100%**

Recommended Resources

1. Rabaey, J.M., Chandrakasen, A.P. and Nikolic, B., Digital Integrated Circuits – A Design perspective, Pearson Education (2007) 2nd ed.
2. Kang, S. and Leblebici, Y., CMOS Digital Integrated Circuits – Analysis and Design, Tata McGraw Hill
3. J P Uyemura, CMOS Circuit Design, Springer
4. Weste, N.H.E. and Eshraghian, K., CMOS VLSI Design: A Circuits and Systems Perspective, eddision Wesley (1998) 2nd ed.
5. Baker, R.J., Lee, H. W. and Boyce, D. E., CMOS Circuit Design, Layout and Simulation, Wiley - IEEE Press (2004) 2nd ed.
6. Weste, N.H.E., Harris, D. and Banerjee, A., CMOS VLSI Design, Dorling Kindersley (2006) 3rd ed.

Other Resources

1. James D. Plummer, Michael D. Deal, Peter B. Griffin, Silicon VLSI Technology: Fundamentals, Practice and Modeling, Pearson Education, 2009.

Course Designers

1. Dr. M. Durga Prakash,. Asst. Professor. Dept. Of ECE. SRM University - AP

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CMOS Digital IC Design Lab

Course Code	VLS 511L	**Course Category**	Core Course (CC)	**L**	**T**	**P**	**C**
				0	0	1	1
Pre-Requisite Course(s)		**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	ECE	**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. To learn the schematic and layout of CMOS logic circuits.
2. To understand the CMOS combinational and dynamic logic circuits
3. To apply the performance of CMOS logic circuits.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Understand the schematic and layout of CMOS logic circuits.	2	85%	80%
Outcome 2	Design CMOS combinational and dynamic logic circuits	3	80%	75%
Outcome 3	Analyze the performance of CMOS logic circuits.	3	80%	75%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	2	3	2	1		1	2	2	2	3	1	2	2
Outcome 2	2	3	2	1		1	2	2	2	3	2	2	2
Outcome 3	2	3	2	1		1	2	2	2	3	2	2	2
Average	**2**	**3**	**2**	**1**		**1**	**2**	**2**	**2**	**3**	**2**	**2**	**2**

Course Unitization Plan

Session	Description of Experiment	Required Contact Hours	CLOs Addressed	Reference Used
1.	Familiarization with schematic circuit simulation and layout entry using Cadence Tool	2	1	1,2
2	DC transfer Characteristics of Inverters	2	1	1,2
3	Transient response, Calculating propagation delays, rise and fall times	4	1	1
4	Circuit design of inverters, complex gates with given constraints	4	2	1
5	Circuit Simulation and Performance Estimation	4	2	1
6	Layouts of CMOS circuits	4	2	1
7	Layout optimization, Design Rule Check (DRC), Electrical Rule Check (ERC)	2	2	1
8	Comparison of Layout Vs. Schematics	2	2.3	4
9	CMOS digital circuit extraction	2	2,3	4
10	Mini Capstone Project	4	2,3	
Total Contact Hours		**30**		

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)			End Semester Exam (50%)
		Experiments (20%)	Record / Observation Note (10%)	Viva + Model (20%)	
Level 1	Remember	40%	60%	50%	40%
	Understand				
Level 2	Apply	40%	40%	40%	40%
	Analyse				
Level 3	Evaluate	20%	10%	10%	20%
	Create				
Total		**100%**	**100%**	**100%**	**100%**

Recommended Resources

1. Kang, S. and Leblebici, Y., CMOS Digital Integrated Circuits – Analysis and Design, Tata
2. McGraw Hill (2008) 3rd ed.
3. J P Uyemura, CMOS Circuit Design, Springer

Other Resources

1.

Course Designers

1. Dr. M. Durga Prakash, Assistant Professor, Department of ECE, SRM University AP.

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Guntur District, Mangalagiri, Andhra Pradesh – 522240.

Embedded Programming

Course Code	VLS 512	**Course Category**	Core Course (CC)	**L**	**T**	**P**	**C**
				3	0	0	3
Pre-Requisite Course(s)		**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	ECE	**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. Understand the basics of Embedded Systems.
2. Learn the ARM architecture, instruction set and its assembly programming.
3. Learn to develop C programs for ARM processors and interfacing the peripherals.
4. Understand the software architectures used in Embedded Systems.
5. Learn the embedded system security including the network security.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Understand and explain the basics of Embedded Systems.	2	80%	70%
Outcome 2	Understand the ARM Cortex M Architecture, instruction set and do ARM assembly & C programming.	3	80%	70%
Outcome 3	Understand the architecture used in Embedded Softwares	2	80%	70%
Outcome 4	Understand the RTOS concepts and develop RTOS applications for ARM Microcontrollers.	3	80%	70%
Outcome 5	Understand various Embedded System Attacks & its security measures.	2	80%	70%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	2	2	1				1		1	1	1	1
Outcome 2	3	3	3	1				1		2	2	2	2
Outcome 3	3	1	2	1				1		1	2	2	2
Outcome 4	3	1	3	1				1		2	2	2	2
Outcome 5	3	1	2	1				1		2	2	2	2
Average	3	1	2	1				1		2	2	2	2

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit 1	**OVERVIEW**	**9**		
1	Embedded System Case Studies	2	1	1,3
2	Introduction to Embedded Systems	2	1	1,3,4
3	Getting to Know the Hardware	2	1	1,3,4
4	Learn How to Communicate	1	1	1,3,4
5	Getting to Know the Processor	1	1	1,3,4
6	Study the External Peripherals	1	1	1,3,4
Unit 2	**ARM REFERENCE ARCHITECTURE**	**9**		
7	ARM Processor Architecture	1	**2**	1,3,4
8	ARM Software Development	1	2	1,3,4
9	ARM Instruction Sets	1	2	1,3,4
10	Getting Started with Embedded Software Development (Tools, Packages, Platforms, etc.)	1	2	1,3,4
11	Your First Embedded Program-Hello, ARM!	1	2	1,3,4
12	The Blinking LED Program	1	2	1,3,4
13	The Role of the Infinite Loop	1	2	1,3,4
14	Compiling, Linking, and Locating	1	2	1,3,4
15	The Build Process	1	2	1,3,4
Unit 3	**SOFTWARE ARCHITECTURE**	**11**		
18	Four types of common architectures	3	3	3
19	Peripherals (drivers)	2	3	3
20	Interrupts (ISR, IVT, pitfalls, etc.)	1	3	3,5
21	Round-Robin	2	3	3,5
22	The Shared Data Problems	2	3	3,5
23	Function-Queue-Scheduling Architecture	1	3	3
Unit 4	**EMBEDDED OPERATING SYSTEM**	**10**		
27	Real-Time Operating Systems	3	4	2,8
28	Interrupt Routines in an RTOS Environment	2	4	2,8
29	Tasks and Task States	3	4	2,8
30	Tasks and Data	2	4	2,8
Unit 5	**EMBEDDED PROGRAMMING AND SECURITY**	**6**		
31	Embedded Systems Attacks: Uniquely Embedded Insecurities	3	5	2
32	Attackers and Assets: Common Firmware Vulnerabilities	2	5	2
33	Java: Concurrency, Pitfalls, and Wireless Applications	1	5	2
	Total Contact Hours	**45**		

Course Unitization Plan - Lab

Session	Description of Experiment	Contact hours required	CLOs Addressed	Reference Used
1	ARM Assembly language program for doing arithmetic operation.	2	2	6,8
2	ARM assembly language program for Memory operations	2	2	6,8
3	ARM Assembly - Interfacing memory mapped peripherals 1. Binary Counter with LEDs 2. Real Time Clock 3. Analog to Digital converter 4. Digital to Analog Converter	4	2	6
4	C Program for peripheral interfacing 1. GPIO 2. Real Time Clock 3. Analog to Digital Converter 4. Digital to Analog Converter	4	2	6
5	C Program for Asynchronous and synchronous serial communication 1. UART 2. I2C/SPI	4	2	6
6	Embedded Ethernet applications	4	2	6
7	Controller Area Network (CAN) interface	2	2	6
8	RTOS Task Management	2	3	8
9	RTOS Inter Task Synchronization and Inter Task communication	4	3	8
10	Mini Capstone Project	2	2,3	
Total Contact Hours		**30**		

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)								End Semester Exam (50%)	
		CLA-1 (15%)		Mid-1 (15%)		CLA-2 (10%)		CLA-III (10%)			
		Th	Prac	Th	Prac	Th	Prac	Th	Prac	Th	Prac
Level 1	Remember	40%		30%		40%		40%		50%	
	Understand										
Level 2	Apply	60%		70%		60%		60%		50%	
	Analyse										
Level 3	Evaluate										
	Create										
Total		100%		100%		100%		100%		100%	

Recommended Resources

1. Barr, Michael, and Anthony Massa. Programming embedded systems: with C and GNU development tools. " O'Reilly Media, Inc.", 2006.
2. Simon, David E. An embedded software primer. Vol. 1. Addison-Wesley Professional, 1999.
3. Edward A. Lee and Sanjit A. Seshia, Introduction to Embedded Systems, A Cyber-Physical Systems Approach, Second Edition, MIT Press, ISBN 978-0-262-53381-2, 2017.
4. Richard Barnett, Sarah Cox, Larry O'Cull, Embedded C programming and the Atmel AVR. 2 edition. Clifton Park, N.Y. : Thomson Delmar Learning (532 p).
5. Wolf, Wayne (2008), Computers as components : principles of embedded computing system design. 2 edition. Amsterdam : Elsevier (507 p).
6. Ata Elahi, Trevor Arjeski, "ARM Assembly Language with Hardware Experiments", Springer, 2015.
7. A.N.Sloss et al., "ARM System Developer's Guide", Morgan Kaufmann Publishers, 2004
8. Richard Barry, "Mastering the FreeRTOS™ Real Time Kernel", Real Time Engineers Ltd 2016

Other Resources

1. Enter Data

Course Designers

1. Dr Ramakrishnan M. Associate Professor, Department of Electronics and Communication Engineering, SRM University – AP.

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Embedded Programming Lab

Course Code	VLS 512L	**Course Category**	Core Course (CC)	**L**	**T**	**P**	**C**
				0	0	1	1
Pre-Requisite Course(s)		**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	ECE	**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. Understand the write the ARM assembly programs accessing the peripherals.
2. Write the C Programs for ARM processors for peripheral interfacing .
3. Write the FreeRTOS .programs for ARM Cortex M Processor.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Develop assembly language program for ARM Cortex M processor.	3	80%	70%
Outcome 2	Develop C programs for ARM Cortex M processor for interfacing internal and external peripherals.	3	80%	70%
Outcome 3	Develop FreeRTOS programs for ARM Cortex M Processor.	3	80%	70%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	2	3	2	1		1	2	2	2	3	1	2	2
Outcome 2	2	3	2	1		1	2	2	2	3	2	2	2
Outcome 3	2	3	2	1		1	2	2	2	3	2	2	2
Average	2	3	2	1		1	2	2	2	3	2	2	2

Course Unitization Plan

Session	Description of Experiment	Contact hours required	CLOs Addressed	Reference Used
1.	ARM Assembly language program for doing arithmetic operation.	2	1	1,2
2	ARM assembly language program for Memory operations	2	1	1,2
3	ARM Assembly - Interfacing memory mapped peripherals 1. Binary Counter with LEDs 2. Real Time Clock 3. Analog to Digital converter 4. Digital to Analog Converter	4	1	1
4	C Program for peripheral interfacing 1. GPIO 2. Real Time Clock 3. Analog to Digital Converter 4. Digital to Analog Converter	4	2	1
5	C Program for Asynchronous and synchronous serial communication 1. UART 2. I2C/SPI	4	2	1
6	Embedded Ethernet applications	4	2	1
7	Controller Area Network (CAN) interface	2	2	1
8	RTOS Task Management	2	2.3	4
9	RTOS Inter Task Synchronization and Inter Task communication	4	2,3	4
10	Mini Capstone Project	2	2,3	
Total Contact Hours		**30**		

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)			End Semester Exam (50%)
		Experiments (20%)	Record / Observation Note (10%)	Viva + Model (20%)	
Level 1	Remember	30%	70%	30%	30%
	Understand				
Level 2	Apply	70%	30%	70%	70%
	Analyse				
Level 3	Evaluate				
	Create				
Total		**100%**	**100%**	**100%**	**100%**

Recommended Resources

1. Ata Elahi, Trevor Arjeski, "ARM Assembly Language with Hardware Experiments", Springer, 2015.
2. A.N.Sloss et al., "ARM System Developer's Guide", Morgan Kaufmann Publishers, 2004
3. Richard Barry, "Mastering the FreeRTOS™ Real Time Kernel", Real Time Engineers Ltd 2016

Other Resources

1.

Course Designers

1. Dr. Ramakrishnan Associate Professor, Department of ECE, SRM University AP.

SRM University *AP*, Andhra Pradesh
Neerukonda, Mangalagiri Mandal,
Guntur District, Mangalagiri, Andhra Pradesh – 522240.

VLSI Technology

Course Code	VLS 513	**Course Category**	Core Course (CC)	**L**	**T**	**P**	**C**
				3	0	1	4
Pre-Requisite Course(s)		**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	ECE	**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. To study the various processes of IC fabrication.
2. To study the device fabrication process.
3. To understand various issues of defects and stresses in the films.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	**Bloom's Level**	**Expected Proficiency Percentage**	**Expected Attainment Percentage**
Outcome 1	Outline the basics of semiconductor crystal properties	2	80%	75%
Outcome 2	Identify the fundamentals of IC fabrication	3	80%	75%
Outcome 3	Illustrate the different methods involved in VLSI fabrication process.	4	80%	75%
Outcome 4	Appreciate the advanced methods involved in IC fabrication.	4	80%	75%
Outcome 5	Build the knowledge of process integration-of devices	4	80%	75%
Outcome 6	Build the knowledge of Packaged the devices	4	80%	75%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	**Program Learning Outcomes (PLO)**												
	Engineering Knowledge	**Design / Development of Solutions**	**Conduct Investigations of Complex Problems**	**Modern Tools and ICT Usage**	**The Engineer and Society**	**Environment and Sustainability**	**Ethics**	**Individual and Teamwork Skills**	**Communication Skills**	**Life-long Learning**	**PSO 1**	**PSO 2**	**PSO 3**
Outcome 1	3	1	1	2	2	2	2	2	2	2	2	3	1
Outcome 2	3	1	1	2	2	2	2	2	2	2	2	3	1
Outcome 3	2	3	3	3	3	3	2	3	2	3	3	2	3
Outcome 4	2	3	3	3	3	3	3	3	1	3	3	2	3
Outcome 5	2	3	3	3	3	3	3	3	2	3	3	2	3
Outcome 6	2	3	3	3	3	3	3	3	1	3	3	2	3

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOsAddressed	References
Unit 1	**Clean Room Environment and Wafer Preparation**	**10**		
	Crystal Structure of a solid	1	1	1,2
	Defects in materials	1	1	1,2
	Types of clean room, Contamination in clean room	2	1,2	1,2
	Electronic Grade Silicon, Czochralski crystal growing	2	1,2	1,2,4,6
	Silicon Shaping	2	1,2	
	Wafer cleaning processes and wet chemical etching techniques	2	1,2	1,2,4,6
Unit 2	**Oxidation, Diffusion, and Implantation**	**12**		
	Kinetics of Silicon dioxide growth both for thick, thin, and ultrathin films	3	2,3	1,2
	Oxidation Techniques and Systems Models of Diffusion in Solids	2	2,3	1,2
	Defects due to oxidation	2	1,2,3	1,2
	Solid State diffusion modelling and technology	2	1,2,3	1,2
	Implantation Equipment, Principles, techniques and applications	2	2,3	1,2
	Removal of implant damage	1	2,3	
Unit 3	**Epitaxial Growth, Metallization**	**12**		
	CVD and MBE	3	2,3	1,2,3
	Defects in Epitaxial Layer Dielectric Deposition	2	2,3	1,2,3
	PECVD and Rapid Thermal Annealing	2	2,3,4	1,2,3
	E-beam evaporation	2	2,3,4	1,2,3
	Sputtering and Thermal Evaporation	2	2,3	1,2,3
	Etching	1	2,3,4	1,2,3
Unit 4	**Lithography**	**6**		
	Optical Lithography	2	2,3,4	1,2,5
	E-beam lithography	2	2,3,4	1,2,5
	X-ray	1	2,3,4	1,2,5
	Other Lithography techniques	1	2,3,4	1,2,5
Unit 5	**Fabrication and Packaging**	**6**		
	Fabrication of MOSFET	2	3,4,5	1,2,5
	Process to Package a chip (Dicing, Attaching, wire bonding, Chip package header)	2	2,3,4	1,2,5
	Fabrications of other devices	2	2,3,4	1,2,5
	Total	**46**		

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)				End Semester Exam (50%)
		CLA-1 20%	Mid-1 20%	CLA-2 20%	CLA-3 20%	
Level 1	Remember	40%	40%	20%	30%	30%
	Understand					
Level 2	Apply	40%	40%	40%	30%	50%
	Analyse					
Level 3	Evaluate	20%	20%	40%	40%	20%
	Create					
Total		100%	100%	100%	100%	100%

Recommended Resources

1.

Other Resources

1.

Course Designers

1. Dr. Manas Ranjan Tripathy. Asst. Professor. Dept. Of ECE. SRM University – AP

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Machine Learning Techniques

Course Code	AML 501	**Course Category**	Core Course (CC)	**L**	**T**	**P**	**C**
				3	0	0	3
Pre-Requisite Course(s)		**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	CSE	**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. Introduce Machine Learning and various task involved in the pipeline of machine learning application development.
2. Understand a wide variety of regression, classification and clustering algorithms.
3. Apply the algorithms to a real-world problem, optimize the models learned and report on the expected accuracy that can be achieved by applying the models.
4. Learn the rapid advances in Machine Learning and able to understand the research articles

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Demonstrate the phases of machine learning application development.	2	75%	75%
Outcome 2	Describe the learning algorithms.	2	75%	70%
Outcome 3	Explain the techniques to deal with data and its dimension.	2	70%	65%
Outcome 4	Develop speech recognition, object recognition and classification models using machine learning algorithms	5	70%	65%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	2	2	2							2		
Outcome 2	3	2	2	3							2		
Outcome 3	3	3	3	3							2		
Outcome 4	3	2	2	2							3		
Outcome5	3	2	3	2							3		
Average	3	2	2	3							2		

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
	UNIT I:	**10**		
1.	**Introduction:** Introduction to Machine Learning	1	1	1
2.	Different types of learning	1	1	1
3.	Hypothesis space and inductive bias, Evaluation	1	1	1
4.	Training and test sets, cross validation	1	3	2
5.	Concept of over fitting, under fitting, Bias and Variance.	1	3	2
6.	Linear Regression: Introduction	1	2	3
7.	Linear Regression: Simple	1	2,4	3
8.	Linear Regression: Multiple	1	2,4	3
9.	Polynomial regression	1	2,4	3
10.	Evaluating regression fit	1	2,4	3
	UNIT II:	**12**		
11.	**Decision tree learning:** Introduction, Decision tree representation	1	2,4	1
12.	appropriate problems for decision tree learning, the basic decision tree algorithm	1	2,4	1
13.	hypothesis space search in decision tree learning, inductive bias in decision tree learning,	1	2,4	1
14.	issues in decision tree learning, Python exercise on Decision Tree.	1	2,4	1
15.	**Instance based Learning:** K nearest neighbour, numerical problem	1	2,4	1
16.	the Curse of Dimensionality, Feature selection, forward search, backward search,	1	2,4	1
17.	Univariate and Multivariate feature selection approaches	1	2,4	1
18.	Feature selection techniques	1	2,4	1
19.	Feature reduction: Principal Component Analysis	1	2,4	1
20.	Feature reduction: Principal Component Analysis	1	2,4	1
21.	Python exercise on kNN and PCA	1	2,4	1
22.	**Recommender System:** Content based system, Collaborative filtering based	1	2,4	4
	UNIT III:	**7**		
23.	**Probability and Bayes Learning:** Probability and classification, Bayesian Learning,	1	2	1
24.	Python exercise on Naïve Bayes, Logistic Regression.	2	2,4	1
25.	**Support Vector Machine:** Introduction, the Dual formulation,	1	2,4	1
26.	Maximum margin with noise, nonlinear SVM and Kernel function, solution to dual problem	3	2,4	1
	UNIT IV:	**8**		
27.	**Artificial Neural Networks:** Introduction,	1	2,4	2
28.	Biological motivation	1	2,4	2
29.	ANN representation	1	2,4	2
30.	appropriate problem for ANN learning,	1	2,4	2
31.	Peceptron	1	2,4	2
32.	multilayer networks	1	2	1
33.	back propagation algorithm	2	2	1
	UNIT V:	**8**		
34.	**Ensembles:** Introduction, Bagging and boosting, Random Forest	2	2,4	3
35.	Discussion on some research papers	1	2,4	3
36.	Discussion on some research papers	1	2,4	3
37.	**Clustering:** Introduction, K-mean clustering	2	2,4	3
38.	agglomerative hierarchical clustering,	1	2,4	3
39.	Python exercise on k-mean clustering.	1	2,4	3
	Total contact hours	**45**		

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)				End Semester Exam (50%)
		CLA-1 (10%)	Mid-1 (15%)	CLA-2 (10%)	Mid -2 (15%)	
Level 1	Remember	30%	30%	30%	30%	30%
	Understand					
Level 2	Apply	40%	40%	40%	40%	40%
	Analyse					
Level 3	Evaluate	30%	30%	30%	30%	30%
	Create					
Total		**100%**	**100%**	**100%**	**100%**	**100%**

Recommended Resources

1. Machine Learning. Tom Mitchell. First Edition, McGraw- Hill, 1997.
2. Alpaydin, Ethem. Introduction to machine learning. MIT press, 2020.
3. Kevin P. Murphy, "Machine Learning: A Probabilistic Perspective", MIT Press, 2012.
4. Christopher Bishop, "Pattern Recognition and Machine Learning" Springer, 2007

Other Resources

1.

Course Designers

1. Dr. Jatindra Kumar Dash, Associate Professor, Computer Science and Engineering, SRM University – AP.

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Neerukonda, Mangalagiri Mandal,
Guntur District, Mangalagiri, Andhra Pradesh – 522240.

Machine Learning Techniques Lab

Course Code	AML 501L	**Course Category**	Core Course (CC)	**L**	**T**	**P**	**C**
				0	0	3	2
Pre-Requisite Course(s)		**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	CSE	**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. Introduce Machine Learning and various task involved in the pipeline of machine learning application development.
2. Understand a wide variety of regression, classification and clustering algorithms.
3. Apply these algorithms to a real-world problem, optimize the models learned and report on the expected accuracy that can be achieved by applying the models.
4. Learn the rapid advances in Machine Learning and able to understand the research articles.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Expertise to use the packages NumPy, Pandas and matplotlib	2	75%	75%
Outcome 2	Able to analyse the data and predictions using statistical techniques	2	75%	70%
Outcome 3	Develop classification models for the prediction of class label	2	70%	65%
Outcome 4	Develop perceptron-based classification models for classification	6	70%	65%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	2	2	3							2		
Outcome 2	3	3	1	3							2		
Outcome 3	3	3	3	3							2		
Outcome 4	3	2	2	2							3		
Outcome5	3	2	3	2							3		
Average	3	2	2	3							2		

Course Unitization Plan

Sl. No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
1.	Basic exercises on Python Machine Learning Packages such as Numpy, Pandas and matplotlib	4	1	1,2
2.	Given a dataset. Write a program to compute the Covariance, Correlation between a pair of attributes. Extend the program to compute the Covariance Matrix and Correlation Matrix.	2	2	2
3.	Given a set of sample points in N dimensional feature space. Write a program to fit the points with a hyper plane using Linear Regression. Calculate sum of residual error.	2	2	4
4.	Write a program that provides option to compute different distance measures between two points in the N dimensional feature space. Consider some sample datasets for computing distances among sample points.	2	2	4
5.	Write a program to demonstrate the working of the decision tree based ID3 algorithm. Use an appropriate data set for building the decision tree and apply this knowledge to classify a new sample.	2	3	4
6.	Write a program to implement k-Nearest Neighbour algorithm to classify the iris data set. Print both correct and wrong predictions. Python ML library classes can be used for this problem.	2	3	4
7.	Write a program to implement feature reduction using Principle Component Analysis	2	3	4
8.	Write a program to implement the naïve Bayesian classifier for a sample training data set stored as a .CSV file. Compute the accuracy of the classifier, considering few test data sets.	2	3	4
9.	Given a dataset for classification task. Write a program to implement Support Vector Machine and estimate it test performance.	2	3	4
10.	Write a program to implement perceptron for different learning task	2	4	4
11.	Write programs to implement ADALINE and MADALINE for given learning task.	2	4	2
12.	Build an Artificial Neural Network by implementing the Back propagation algorithm and test the same using appropriate data sets.	4	4	2
13.	Write a program to implement K means clustering algorithm. Select your own dataset to test the program. Demonstrate the nature of output with varying value of K.	2	3	2
	Total contact hours	**30**		

Learning Assessment

Bloom's Level of Cognitive Task		Lab Performance (30%)	Viva (20%)
Level 1	Remember	30%	30%
	Understand		
Level 2	Apply	40%	40%
	Analyse		
Level 3	Evaluate	30%	30%
	Create		
Total		100%	100%

Recommended Resources

1. Machine Learning. Tom Mitchell. First Edition, McGraw- Hill, 1997.
2. Alpaydin, Ethem. Introduction to machine learning. MIT press, 2020.
3. Kevin P. Murphy, “Machine Learning: A Probabilistic Perspective”, MIT Press, 2012.
4. Christopher Bishop, “Pattern Recognition and Machine Learning” Springer, 2007.

Other Resources

1. Enter Data

Course Designers

1. Dr. Jatindra Kumar Dash, Associate Professor, Computer Science and Engineering, SRM University – AP.

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English for Research Paper Writing

Course Code	EGL 501	**Course Category**	AEC	**L**	**T**	**P**	**C**
				1	0	0	1
Pre-Requisite Course(s)		**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	English	**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. Understand the Structure of a Research Paper
2. Familiarize students with the different types of research & methodologies.
3. Develop fundamental proofreading skills to identify and correct common grammatical errors.
4. Guide students in creating clear thesis statements and research questions to shape their papers.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Identify and recall the key components of a research paper, including abstracts, introductions, methods, results, discussions, and conclusions.	1,2	75%	75%
Outcome 2	Interpret the structure and organization of research papers, recognizing the role each section plays in conveying information.	2	75%	75%
Outcome 3	Analyze the effectiveness of thesis statements and research questions in guiding the development of a research paper.	3	75%	75%
Outcome 4	Generate clear and concise sentences, paragraphs, and sections that conform to academic writing standards.	3	75%	75%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1		1				3	3	3	3				
Outcome 2		1				3	3	3	3				
Outcome 3		1				3	3	3	3				
Outcome 4		1				3	3	3	3				
Average		1				3	3	3	3				

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit 1	**Planning & Preparation**	**3**		
	What is research & the need for research	1	1,2	1,2
	Planning a manuscript	2	1,2	1,2
			1	1,2
Unit 2	**The Key to Good Writing**	**3**		
	Structuring a paragraph	2	1,2	1,2
	Sequencing a paragraph	1	1,2	1,2
Unit 3	**Being Concise**	**3**	1,2	1,2
	The steps to being concise	2	1,2	1,2
	Redundancy Vs Conciseness	1	1,2	1,2
Unit 4	**The Basic Components**	**3**		
	Abstract & Introduction	2	3	1,2
	Basic Formats	1	1,2	1,2
			1,3	1,2
Unit 5	**Practical Implementation**	**3**		
	Presentation of a paper	3	1,2,3,4	1,2
Total Contact Hours		**15**		

Learning Assessment

Bloom's Level of Cognitive Task		**Continuous Learning Assessments (50%)**								**End Semester Exam (50%)**	
		CLA-1 (10%)		**CLA -2 (10%)**		**CLA-3 (20%)**		**Mid-1 (15%)**			
		Th	**Prac**	**Th**	**Prac**	**Th**	**Prac**	**Th**	**Prac**	**Th**	**Prac**
Level 1	Remember	30%		20%		30%		50%		50%	
	Understand										
Level 2	Apply	70%		80%		70%		50%		50%	
	Analyse										
Level 3	Evaluate										
	Create										
Total		**100%**		**100%**		**100%**		**100%**		**100%**	

Recommended Resources

1. Wallwork Adrian. (2016). English for Writing Research Papers. New York: Springer.
2. Dudley Evans, T. (1998). Developments in English for Specific Purposes: A multidisciplinary approach. U.K: Cambridge University Press

Other Resources

1. Hutchinson, T., & Waters, A. (1987). English for Specific Purposes: A learner-centered approach. U.K: Cambridge University Press
2. Raman, Meenakshi, and Sangeetha Sharma. (2008). Technical Communication: English Skills for Engineers. New Delhi: Oxford University Press
3. Trimble, Louis. English for Science and Technology - A Discourse Approach. (1985). Cambridge: Cambridge University Press
4. Williams, Phil. Advanced Writing Skills for Students of English. (2018). Brighton: Rumian Publishing.
5. Wilson, Paige and Teresa Ferster Glazier. (2013). The Least You Should Know About English: Writing Skills, Form C (11th Edition). Boston: Cengage Learning.

Course Designers

1. Dr. Srabani Basu

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Fundamentals of Business Innovation and Entrepreneurship

Course Code	VLS 548	**Course Category**	RDIP	**L**	**T**	**P**	**C**
				1	0	0	1
Pre-Requisite Course(s)		**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	ECE	**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. To Understand the principles of business, innovation and project management and design thinking.
2. To impart Design Thinking which plays key role for winning in the IoT space.
3. To imbibe the spirit of startup culture and be innovative in thinking.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Understand the fundamentals of business.	2	80%	70%
Outcome 2	Understand the process of taking innovation to successful product/service.	2	80%	70%
Outcome 3	Understand the management of large projects.	3	80%	70%
Outcome 4	Think of innovative IoT solutions to fill the business gaps.	2	80%	70%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	1	1	2			1	1	1	1			1	2
Outcome 2	1	1	2			1	1	1	2			1	2
Outcome 3	1	1	2	1	1	1	1	1	1	1	1	1	2
Outcome 4	1	2	2	1	1	1	1	1	2	1	1	1	2
Average	1	1	2	1	1	1	1	1	2	1	1	1	2

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit 1	**Introduction to Business**	3		
1	What is a Business Model-The Business Fundamentals and its types	1	1	1,2
2	The Business Owners/Managers-Your Goals & Planning- Your Business Finances	1	1	1,2
3	The Operational Systems & Processes- Your Team- The Brand- Sales & Marketing Plans- Customer Experience	1	1	1,2
	UNIT II : What is Innovation	3		
4	Are you innovative - What are the characteristics of Innovators - Why does Innovation matters - What kinds of innovation Exist-Social Innovation-	1	2	3,4
5	Innovation Management Process-Stages of successful Innovation-Idea Generation and Mobilization- Advocacy and Screening- Experimentation- Commercialization- Diffusion and Implementation.	2	2	3,4
UNIT III	**Business Innovation**	3		
6	Models of Business Innovation- Business Model- and new Business Models	2	2	3,4
7	The 9 most successful Business models of today	1	2	3,4
UNIT IV	**Project Management**	4		
8	Four Phases of project Management-Planning	2	3	5
9	Build up-Implementation-Closeout.	2	3	5
UNIT V	**Design Thinking and IoT space**	3		
10	Design Thinking -The key to winning in the IoT space.	1	4	6
11	5 steps of Design Thinking for your IoT project	2	4	6
12	Case studies-IoT Business Models that are transforming Industries.	1	4	6
	Total Contact Hours	**16**		

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)								End Semester Exam (50%)	
		CLA-1 (15%)		Mid-1 (15%)		CLA-2 (10%)		CLA-III (10%)			
		Th	Prac	Th	Prac	Th	Prac	Th	Prac	Th	Prac
Level 1	Remember	80%		80%		80%		80%		80%	
	Understand										
Level 2	Apply	20%		20%		20%		20%		20%	
	Analyse										
Level 3	Evaluate										
	Create										
Total		100%		100%		100%		100%		100%	

Recommended Resources

1. Lawrence J. Gitman, Carl McDaniel (Jr.), Amit J. Shah, Monique Reece, Linda Koffel, Bethann Talsma, James C. Hyatt, "Introduction to Business", OpenStax, Rice University, 2018.
2. William Nickels, James Mchugh, Susan Mchugh, "Understanding Business", McGraw-Hill Education, 2018.
3. Matt Ridley, " How Innovation Works: And Why It Flourishes in Freedom", Springer Berlin Heidelberg, 2020.
4. Larry Keeley, Helen Walters, Ryan Pikkel, Brian Quinn, " Ten Types of Innovation: The Discipline of Building Breakthroughs ", wiley Publications, 2013.
5. " HBR Guide to Project Management", Harvard Business Review, 2013.
6. Maciej Kranz, "Building the Internet of Things: Implement New Business Models, Disrupt Competitors, Transform Your Industry", wiley Publications, 2016.

Other Resources

1.

Course Designers

1. Dr. Associate Professor, Department of Electronics and Communication Engineering, SRM University – AP.

SRM University *AP*, Andhra Pradesh
Neerukonda, Mangalagiri Mandal,
Guntur District, Mangalagiri, Andhra Pradesh – 522240.

VLSI Testing and Verification

Course Code	VLS 521	**Course Category**	Core Course (CC)	**L**	**T**	**P**	**C**
				3	0	0	3
Pre-Requisite Course(s)	ENG 211 ECE 320	**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department		**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. (To ensure Quality and Reliability): As VLSI circuits become more complex and denser, the likelihood of defects and errors increases. Testing and verification techniques are employed to ensure that the fabricated chips meet the desired specifications and are free from manufacturing defects. This is crucial to ensure the overall quality and reliability of the integrated circuits used in various electronic devices.
2. (To detect and Fix Design Errors): During the design phase of VLSI circuits, errors and bugs can be introduced inadvertently. Proper testing and verification processes help identify these design errors early in the development cycle. This allows designers to correct the mistakes before the chips are manufactured; thus, saving time and costs associated with rework.
3. (Functional Verification): VLSI circuits are designed to perform specific functions. This subject is focused on verifying that these functions are correctly implemented and that the chip behaves as intended under various operating conditions.
4. (Performance Analysis): VLSI Testing and Verification also involve assessing the performance of the integrated circuits. This includes verifying that the chips meet the required speed, power, and area constraints specified during the design phase.
5. (To know about the Test Methodologies and Techniques): This subject will also cover various test methodologies and techniques used to evaluate the performance and functionality of VLSI circuits. This includes design for testability (DFT), built-in self-test (BIST), automatic test pattern generation (ATPG), and scan-based testing, among others.
6. (Fault Models and Test Coverage): Understanding and dealing with different fault models are essential for designing effective tests to identify potential defects in VLSI circuits. This subject will cover various fault models and techniques to achieve high test coverage.
7. (Manufacturability and Yield Enhancement): Testing and verification are critical for assessing the manufacturability of VLSI circuits and improving yield during the chip fabrication process. A higher yield means fewer defective chips, leading to cost savings and better overall productivity.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	have a solid understanding of testing methodologies, verification techniques, and design-for-testability principles	2	80%	70%
Outcome 2	acquire confidence to work on real-world projects, use industry-standard tools, and simulate various testing scenarios	3	80%	70%
Outcome 3	gain insights into the current trends and challenges in VLSI Testing and Verification, such as dealing with increased complexity, power constraints, and manufacturing defects	4	75%	65%
Outcome 4	be able to explore career opportunities in the semiconductor industry, particularly in roles related to design verification, validation, and test engineering	4	70%	60%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	2	2	2	2	2	1	3	3	3	3	2	2	2
Outcome 2	3	2	3	2	2	1	2	2	3	3	2	3	3
Outcome 3	3	2	3	2	2	1	3	2	3	3	2	3	3
Outcome 4	3	2	2	2	2	1	3	2	3	3	3	3	2
Average	**3**	**2**	**3**	**2**	**2**	**1**	**3**	**2**	**3**	**3**	**2**	**3**	**3**

Course Unitization Plan

Unit No.	Description of Topic	Required Contact Hours	CLOs addressed	References Used
Unit 1	**INTRODUCTION TO VLSI TESTING**	**7**	1, 3	1, 2
	VLSI design flow	1		
	Overview of Verification and Testing			
	Need of pre-silicon verification			
	Need of post-silicon validation and debug			
	VLSI Testing needs and challenges	1		
	Possible Outcome of Testing			
	Stages of IC Product			
	Types of Testing: Implicit, Explicit			
	Production Test	1		
	Characterization Test	1		
	Reliability Test	1		
	Test Quality Measures	1		
	Yield and defects			
	Scope of testing and verification in VLSI design process	1		
	Issues in test and verification of complex chips			
Unit 2	**FAULT MODELING AND FAULT SIMULATION**	**12**	1, 3	3, 4, 7, 8
	Overview of Defect, Fault, Error, Failure	1		
	Random and Systematic defects			
	Overview of Test pattern, Test Set, Test Length, Fault Coverage			
	Importance of Fault modeling			
	Introduction to Fault models	1		
	Single stuck-at-fault model			
	Fanout stem and branch for Stuck-at-fault model			
	Multiple stuck at fault	1		
	Bridging faults			
	Bridging fault models: Wired-OR, Wired-AND, A-Dominant	2		
	Feedback bridging faults	2		
	Fanout Stem and Branch for Bridge Fault			

	Permanent and Transient Bridge Fault			
	Delay fault and its detection	2		
	Delay fault models Introduction			
	Path delay fault: Falling transition, Rising transition			
	Transition delay fault: Slow-to-rise (STR) and slow-to-fall (STF)	1		
	Overview of Transistor level or Switch level fault model	1		
	Stuck-open fault			
	Stuck-short fault			
	Fault Simulation Overview	1		
	Yield and Fault Equivalence			
Unit 3	**TESTABILITY MEASURES AND ANALYSIS**	**6**	1, 3, 4	2, 7
	Introduction and need of testability measures	1		
	Testability Components: Controllability and Observability			
	Overview of Testability Analysis			
	Topology-based Analysis	2		
	SCOAP: Combinational Controllability and Combinational Observability			
	Probability-based Analysis	2		
	COP: Combinational Controllability and Combinational Observability			
	High-level Analysis	1		
Unit 4	**ATPG AND DESIGN FOR TESTABILITY METHODS**	**14**	1, 2, 3	5, 6, 7, 8, 9
	Test pattern generation Overview: Random and Deterministic	1		
	Automatic test pattern generation: Complete and Incomplete ATPG			
	Combinational ATPG Introduction	2		
	Boolean Difference Method			
	SAT	1		
	Path-sensitization Method	2		
	Single Path Sensitization			
	Multiple Path Sensitization			
	D Algorithm	1		
	PODEM	1		
	FAN	1		
	Sequential ATPG Introduction	3		
	Scan design			
	Issues in Scan Design			
	Test interface and boundary scan			
	Iddq testing			
	Delay fault testing	2		
	Built-in Self-Test			
Unit 5	**VLSI DESIGN VERIFICATION**	**6**	3, 4	7, 8, 10
	Design verification techniques: Introduction	1		
	Techniques based on simulation approach			
	Techniques based on analytical approach	1		
	Techniques based on formal approach	1		
	Functional verification	3		
	Timing verification			
	Formal verification			
Total Contact Hours: 45				

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (60%)				End Semester Exam (40%)
		CLA-1 (15%)	Mid-1 (15%)	CLA-2 (10%)	CLA-3 (20%)	
Level 1	Remember	65%	50%	45%	60%	50%
	Understand					
Level 2	Apply	35%	50%	55%	40%	50%
	Analyse					
Level 3	Evaluate					
	Create					
Total		**100%**	**100%**	**100%**	**100%**	**100%**

Recommended Resources

1. L.T. Wang, C.W. Wu, and X. Wen, "VLSI Test Principles and Architectures", Morgan Kaufmann, 2006
2. M.L. Bushnell and V.D. Agrawal, "Essentials of electronic testing," Kluwer Academic Publishers, 2000
3. George W. Zobrist, VLSI Fault Modeling and Testing Techniques (VLSI Design Automation Series), Praeger Publishers Inc, 1993
4. RL Wadsack, "Fault modeling and logic simulation of CMOS and MOS integrated circuits" Bell System
5. Technology, 1978
6. Hideo Fujiwara, Logic testing and design for testability, MIT Press, 1985
7. M. Abramovici, M. A. Breuer and A.D. Friedman, "Digital systems testing and testable design," IEEE Press,1994
8. P. K. Lala, "Digital Circuits Testing and Testability", Academic Press
9. Stephan Eggersgluss and Rolf Drechsler, High Quality Test Pattern Generation and Boolean Satisfiability, Springer, 2012
10.
11. P.H. Bardell, W.H. McAnney, and J. Savior, "Built-in Test for VLSI: Pseudorandom Techniques," Wiely Interscience, 1987
12. Khosrow Golshan, Physical Design Essentials: An ASIC Design Implementation Perspective, Springer, 2007

Other Resources

1. Enter Data

Course Designers

1. Dr. Swagata Samanta, Assistant Professor, Department of Electronics & Communication Engineering, SRM University – AP

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VLSI Testing and Verification Lab

Course Code	VLS 521L	**Course Category**	Cor Course (CC)	**L**	**T**	**P**	**C**
				0	0	1	1
Pre-Requisite Course(s)	ENG 211 L ECE 320 L	**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	ECE	**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. (To ensure Quality and Reliability): As VLSI circuits become more complex and denser, the likelihood of defects and errors increases. Testing and verification techniques are employed to ensure that the fabricated chips meet the desired specifications and are free from manufacturing defects. This is crucial to ensure the overall quality and reliability of the integrated circuits used in various electronic devices.
2. (To detect and Fix Design Errors): During the design phase of VLSI circuits, errors and bugs can be introduced inadvertently. Proper testing and verification processes help identify these design errors early in the development cycle. This allows designers to correct the mistakes before the chips are manufactured; thus, saving time and costs associated with rework.
3. (Functional Verification): VLSI circuits are designed to perform specific functions. This subject is focused on verifying that these functions are correctly implemented and that the chip behaves as intended under various operating conditions.
4. (Performance Analysis): VLSI Testing and Verification also involve assessing the performance of the integrated circuits. This includes verifying that the chips meet the required speed, power, and area constraints specified during the design phase.
5. (To know about the Test Methodologies and Techniques): This subject will also cover various test methodologies and techniques used to evaluate the performance and functionality of VLSI circuits. This includes design for testability (DFT), built-in self-test (BIST), automatic test pattern generation (ATPG), and scan-based testing, among others.
6. (Fault Models and Test Coverage): Understanding and dealing with different fault models are essential for designing effective tests to identify potential defects in VLSI circuits. This subject will cover various fault models and techniques to achieve high test coverage.
7. (Manufacturability and Yield Enhancement): Testing and verification are critical for assessing the manufacturability of VLSI circuits and improving yield during the chip fabrication process. A higher yield means fewer defective chips, leading to cost savings and better overall productivity.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	have a solid understanding of testing methodologies, verification techniques, and design-for-testability principles	2	80%	70%
Outcome 2	acquire confidence to work on real-world projects, use industry-standard tools, and simulate various testing scenarios	3	80%	70%
Outcome 3	gain insights into the current trends and challenges in VLSI Testing and Verification, such as dealing with increased complexity, power constraints, and manufacturing defects	4	75%	65%
Outcome 4	be able to explore career opportunities in the semiconductor industry, particularly in roles related to design verification, validation, and test engineering	4	70%	60%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)														
	Engineering Knowledge	Problem Analysis	Design and Development	Analysis, Design and Research	Modern Tool and CT Usage	Society and Multicultural Skills	Environment and Sustainability	Moral, and Ethical Awareness	Individual and Teamwork Skills	Communication Skills	Project Management and Finance	Self-Directed and Life Long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	2	2	2	3	2	2	1	3	3	3	2	3	2	2	2
Outcome 2	3	3	2	3	2	2	1	2	2	3	2	3	2	3	3
Outcome 3	3	3	2	3	2	2	1	3	2	3	2	3	2	3	3
Outcome 4	3	2	2	2	2	2	1	3	2	3	2	3	3	3	2
Average	3	3	2	2	2	2	1	3	2	3	2	3	2	3	3

Course Unitization Plan

Exp No.	Experiment Name	Required Contact Hours	CLOs Addressed	References Used
1	Verilog Code for Inverter and Buffer and Test Bench for verification, observation of waveforms, synthesize of code with the technological library, and initial timing verification with gate level simulation	3	2, 3	1
2	Verilog Code for basic gates and universal gates and Test Bench for verification, observation of waveforms, synthesize of code with the technological library, and initial timing verification with gate level simulation	6	2, 3	1
3	Verilog Code for transmission gate and Test Bench for verification, observation of waveforms, synthesize of code with the technological library, and initial timing verification with gate level simulation	2	2, 3	1
4	Verilog Code for flipflops (SR, JK, D, T, Master Slave) and Test Bench for verification, observation of waveforms, synthesize of code with the technological library, and initial timing verification with gate level simulation	6	2, 3, 4	1
5	Verilog Code for serial and parallel adder and Test Bench for verification, observation of waveforms, synthesize of code with the technological library, and initial timing verification with gate level simulation	4	2, 3, 4	1
6	Verilog Code for 4-bit synchronous counter and Test Bench for verification, observation of waveforms, synthesize of code with the technological library, and initial timing verification with gate level simulation	2	2, 3, 4	1
7	Verilog Code for 4-bit asynchronous counter and Test Bench for verification, observation of waveforms, synthesize of code with the technological library, and initial timing verification with gate level simulation	2	2, 3, 4	1
8	Simulation of the schematic of CMOS inverter and buffer performance of the physical verification for the layout of the same using Cadence tool	3	2, 3, 4	1, 2
9	Simulation of the schematic of CMOS NAND and NOR gates and performance of the physical verification for the layout of the same using Cadence tool	2	2, 3, 4	1, 2
Total Contact Hours		**30**		

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)			End Semester Exam (50%)
		Lab Performance (20%)	Model Exam (10%)	Observation Note (20%)	
Level 1	Remember	40%	30%	50%	40%
	Understand				
Level 2	Apply	60%	70%	50%	60%
	Analyse				
Level 3	Evaluate				
	Create				
Total		**100%**	**100%**	**100%**	**100%**

Recommended Resources

1. M. Morris Mano, Digital Design: With an Introduction to the Verilog HDL, VHDL, and System Verilog, Sixth Edition, 2018
2. Sung-Mo Kang and Yusuf Leblebici, Cmos Digital Integrated Circuits, 1996

Other Resources

1.

Course Designers

1. Dr. Swagata Samanta, Assistant Professor, Department of Electronics & Communication Engineering, SRM University – AP.

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Neerukonda, Mangalagiri Mandal,
Guntur District, Mangalagiri, Andhra Pradesh – 522240.

CMOS Analog and Mixed Signal IC Design

Course Code	VLS 522	**Course Category**	Core Course (CC)	**L**	**T**	**P**	**C**
				3	0	0	3
Pre-Requisite Course(s)		**Co-Requisite Course(s)**	VLSI Analog IC Design	**Progressive Course(s)**			
Course Offering Department	ECE	**Professional / Licensing Standards**	IEEE, Microsoft, Oracle, Max Planck Research, Institution of Civil Engineers etc.				

Course Objectives / Course Learning Rationales (CLRs)

1. To understand the fundamental of analog IC Design, including the single-stage amplifiers and Differential Amplifiers
2. To learn the general considerations for Operational Amplifiers designing and performance of various Op-Amp topologies
3. To understand the stability in feedback systems and noise in mixed signal IC design
4. To apply the data converters knowledge gained in the course through hands-on projects that involve the design, simulation, and layout of CMOS analog circuits.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Understand the fundamental of analog IC Design, including the single-stage amplifiers and Differential Amplifiers	2	85%	80%
Outcome 2	Design operational amplifiers and performance of various Op-Amp topologies	3	80%	75%
Outcome 3	Create layout designs for operational amplifier circuits and understand the stability in feedback system and noise performance	3	85%	70%
Outcome 4	Apply theoretical knowledge to real-world analog and digital converter IC design projects	3	80%	70%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	2	2	2	3	2	2	2	3	2	2	3	2
Outcome 2	3	3	3	2	1	2	2	3	3	3	2	3	3
Outcome 3	3	3	3	2	1	2	2	3	2	3	2	3	3
Outcome 4	3	3	3	2	3	3	3	3	3	3	3	3	3
Average	3	3	3	2	2	2	2	3	3	3	2	3	3

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References
Unit 1	**Introduction to Analog Integrated Design**	**10**		
	Models for analog design, body transconductance, Single-stage Amplifiers – CS stage, diode connected load	2	1	1,2
	Current source load and source degeneration Review of CD and CG stages	2	1	1,2
	Cascode stage & folded Cascode concepts	1	1	1,2
	Design of amplifier from specifications Differential Amplifiers	1	1	1,2,4
	MOS differential pair, Small signal operation. half circuit analysis common mode response	2	1,3	
	Differential amplifier with active load, common mode gain, and CMRR. Frequency response of the differential amplifier.	2	1,3	1,2,4
Unit 2	**Operational Amplifiers**	**10**		
	General considerations – performance parameters	1	1,2	1,2
	One-Stage Op amps – Cascode Op-Amps Telescopic Op-Amps	2	1,2	1,2
	Folded Cascode Op-Amps	1	1,2	1,2
	Two-Stage Op amps, Gain boosting	1	1,2	1,2
	Comparison of performance of various Op-Amp topologies	2	1,2	1,2
	Design of Op-Amps from specifications.	2	1,2	1,2
	Review of bode rules	1	1,2	1,2
Unit 3	**Stability In Feedback Systems**	**9**	1,2	1,2
	Problem of instability, Stability condition	1	2,3	1,2,3
	Gain-phase crossovers, phase margin	2	2,3	1,2,3
	Frequency compensation: frequency response of cs amplifier, Miller effect	1	2,3	1,2,3
	Poles in a system, Pole-splitting, miller compensation	2	2,3	1,2,3
	Two-stage Op-Amp - compensation techniques	1	1,3	1,2,3
	Closed-loop stability, optimal phase margin.	2	1,3	1,2,3
Unit 4	**Noise**	**8**		
	MOSFET noise models, types of noise, thermal noise, flicker noise	2	2,4	1,2,5
	Representation of noise in circuits, Noise in single-stage amplifiers	2	2,4	1,2,5
	Integrated Oscillators: Ring oscillators	2	2,4	1,2,5
	LC oscillators – Cross coupled oscillators, VCO.	2	2,4	1,2,5
Unit 5	**Data Converters**	**7**		
	DAC and ADC Specifications, Current Steering DAC	2	2,3,4	1,2,5
	Charge Scaling DAC, Cyclic DAC	1	2,3,4	1,2,5
	Pipeline DAC, Flash ADC	2	2,3,4	1,2,5
	Pipeline ADC, Integrating ADC, Successive Approximation ADC.	2	2,3,4	1,2,5
	Total	**43**		

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)				End Semester Exam (50%)
		CLA-1 (10%)	Mid-1 (15%)	CLA-2 (15%)	CLA-3 (10%)	
Level 1	Remember	40%	60%		50%	30%
	Understand					
Level 2	Apply	60%	40%	20%	50%	60%
	Analyse					
Level 3	Evaluate			80%		10%
	Create					
Total		**100%**	**100%**	**100%**	**100%**	**100%**

Recommended Resources

1. Design of Analog CMOS Integrated Circuits, Behzad Razavi, 2002, Mc GrawHill Edition, ISBN: 0-07- 238032-2.
2. CMOS Circuit Design, Layout and Simulation, R. Jacob Baker, Harry W. Li and David E. Boyce, 2002, IEEE Press, ISBN: 81-203-1682-7.
3. CMOS Mixed-signal Circuit Design, R. Jacob Baker, 2009, IEEE Press, ISBN: 978- 81-265- 1657-5.
4. Analysis and Design of Analog Integrated Circuits, Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, "", 4th edition, 2008, Wiley India Private Limited, ISBN:978-8126515691.
5. Fundamentals of Microelectronics, Behzad Razavi, 2nd Edition, 2013, Wiley, ISBN- 10: 1118156323

Other Resources

1.

Course Designers

1. Dr. M. Durga Prakash. Asst. Professor. Dept. Of ECE. SRM University – AP.

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CMOS Analog and Mixed Signal IC Design Lab

Course Code	VLS 522L	**Course Category**	Core Course (CC)		**L**	**T**	**P**	**C**
					0	0	1	1
Pre-Requisite Course(s)		**Co-Requisite Course(s)**	VLSI Analog IC Design	**Progressive Course(s)**				
Course Offering Department	ECE	**Professional / Licensing Standards**						

Course Objectives / Course Learning Rationales (CLRs)

1. Understand the fundamental of analogue IC Design, including the single-stage amplifiers and Differential Amplifiers
2. Understand the the general considerations for Operational Amplifiers designing and performance of various Op-Amp topologies
3. Understand the stability in feedback systems based circuits for noise in mixed signal IC design
4. Apply the data converters knowledge gained in the course through hands-on projects that involve the design, simulation, and layout of CMOS analog circuits.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Understand the fundamental of analogue IC Design, including the single-stage amplifiers and Differential Amplifiers	2	85%	80%
Outcome 2	Design operational amplifiers and performance of various Op-Amp topologies	3	80%	75%
Outcome 3	Create layout designs for operational amplifier circuits and understand the stability in feedback system and noise performance	3	85%	70%
Outcome 4	Apply practical knowledge to real-world analogue and digital converter IC design projects	3	80%	70%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	2	2	2	3	2	2	2	3	2	2	3	2
Outcome 2	3	3	3	2	1	2	2	3	3	3	2	3	3
Outcome 3	3	3	3	2	1	2	2	3	2	3	2	3	3
Outcome 4	3	3	3	2	3	3	3	3	3	3	3	3	3
Average	3	3	3	2	2	2	2	3	3	3	2	3	3

Course Unitization Plan

Exp No.	Experiment Name	Required Contact Hours	CLOs Addressed	References Used
1	Design an Inverter with given specifications, completing the design flow mentioned below: a. Draw the schematic and verify the following i) DC Analysis ii) Transient Analysis b. Draw the Layout and verify the DRC, ERC c. Extract RC and back annotate the same and verify the Design d. Verify & Optimize for Time, Power and Area to the given constraint.	2	2,3	1,2,3
2	Design the Single stage amplifier circuit with given specifications, completing the design flow mentioned below: a. Draw the schematic and verify the following i) DC Analysis ii) AC Analysis iii) Transient Analysis b. Draw the Layout and verify the DRC, ERC, LVS.	2	3	1,2,3
3	Design the Comparator circuits with given specifications, completing the design flow mentioned below: a. Draw the schematic and verify the following i) DC Analysis ii) AC Analysis iii) Transient Analysis b. Draw the Layout and verify the DRC, ERC, LVS.	2	3	1,2,3
4	Design the Differential amplifier circuits with given specifications, completing the design flow mentioned below: a. Draw the schematic and verify the following i) DC Analysis ii) AC Analysis iii) Transient Analysis b. Draw the Layout and verify the DRC, ERC, LVS.	2	2,3	1,2,3
5	Design the Operational Amplifier circuits with given specifications, completing the design flow mentioned below: a. Draw the schematic and verify the following i) DC Analysis ii) AC Analysis iii) Transient Analysis b. Draw the Layout and verify the DRC, ERC, LVS.	2	3	1,2,3
6	Design the Ring Oscillator circuits with given specifications, completing the design flow mentioned below: a. Draw the schematic and verify the following i) DC Analysis ii) AC Analysis iii) Transient Analysis b. Draw the Layout and verify the DRC, ERC, LVS.	2	3	1,2,3
7	Design the Voltage Controlled Oscillator (VSO) circuits with given specifications, completing the design flow mentioned below: a. Draw the schematic and verify the following i) DC Analysis ii) AC Analysis iii) Transient Analysis b. Draw the Layout and verify the DRC, ERC, LVS.	2	2,3	1,2,3
8	Design the any one Digital to Analog Converter circuits with given specifications, completing the design flow mentioned below: a. Draw the schematic and verify the following i) DC Analysis ii) AC Analysis iii) Transient Analysis b. Draw the Layout and verify the DRC, ERC, LVS.	2	1,2	1,2,3
9	Design the any one Analog to Digital Converter circuits with given specifications, completing the design flow mentioned below: a. Draw the schematic and verify the following i) DC Analysis ii) AC Analysis iii) Transient Analysis b. Draw the Layout and verify the DRC, ERC, LVS.	2	2,3	1,2,3
10	Mini Project	12	2,3	1,2,3
Total Contact Hours		**30**		

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)			End Semester Exam (50%)
		Experiments (20%)	Record / Observation Note (10%)	Viva + Model (20%)	
Level 1	Remember	40%	60%	50%	40%
	Understand				
Level 2	Apply	40%	40%	40%	40%
	Analyse				
Level 3	Evaluate	20%	10%	10%	20%
	Create				
Total		**100%**	**100%**	**100%**	**100%**

Recommended Resources

1. Design of Analog CMOS Integrated Circuits, Behzad Razavi, 2002, Mc GrawHill Edition, ISBN: 0-07- 238032-2.
2. CMOS Circuit Design, Layout and Simulation, R. Jacob Baker, Harry W. Li and David E. Boyce, 2002, IEEE Press, ISBN: 81-203-1682-7.
3. CMOS Mixed-signal Circuit Design, R. Jacob Baker, 2009, IEEE Press, ISBN: 978- 81-265- 1657-5.

Other Resources

1.

Course Designers

1. Dr. M. Durga Prakash. Asst. Professor. Dept. Of ECE. SRM University - AP

SRM University *AP*, Andhra Pradesh
Neerukonda, Mangalagiri Mandal,
Guntur District, Mangalagiri, Andhra Pradesh – 522240.

Mini Project -1

Course Code	VLS 526	Course Category	RDIP	L	T	P	C
				0	0	2	2
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)			
Course Offering Department	ECE	Professional / Licensing Standards					

Course Objectives / Course Learning Rationales (CLRs)

1. Survey the existing research works/literature and analyses them.
2. Demonstrate the skills acquired to solve a technical problem.
3. To have systematic approach to solve the given problem.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Review and analyse the existing research work in a systematic way.	3	80%	70%
Outcome 2	Attain strong technical, domain knowledge in the field of project.	3	80%	70%
Outcome 3	Formulate the complex problem and to have systematic approach for the solution.	2	80%	70%
Outcome 4	Conduct research project	2	80%	70%
Outcome 5	Communicate the technical problems with peers and mentors to move towards appropriate solution.	2	75%	70%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	2	2				2	2	2	1	3	3	2
Outcome 2	3	3	3			1	2	1	2	1	3	3	3
Outcome 3	2	2	3	1	1	1	2	1	2	1	3	2	3
Outcome 4	2	2	3	1	1	1	2	2	3	1	3	2	3
Outcome 5	2	2	3	1	1	1	2	3	3	1	3	2	3
Average	2	2	3	1	1	1	2	2	2	1	3	2	3

Course Unitization Plan

Student is expected to spend minimum 4 hours/week for the Project work.

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)				End Semester Exam (50%)	
		Review -I		Mid Review		Final Review	
		Th	Prac	Th	Prac	Th	Prac
Level 1	Remember		20%		20%		20%
	Understand						
Level 2	Apply		80%		80%		80%
	Analyse						
Level 3	Evaluate						
	Create						
Total			100%		100%		100%

Recommended Resources

1.

Other Resources

1.

Course Designers

1. Dr. M. Durga Prakash, Asst. Professor, Department of Electronics and Communication Engineering, SRM University – AP.

SRM University *AP*, Andhra Pradesh
Neerukonda, Mangalagiri Mandal,
Guntur District, Mangalagiri, Andhra Pradesh – 522240.

Research Methodology and IPR

Course Code	RM 101	**Course Category**	RDIP		**L**	**T**	**P**	**C**
					2	0	0	2
Pre-Requisite Course(s)		**Co-Requisite Course(s)**		**Progressive Course(s)**				
Course Offering Department	Mechanical Engineering	**Professional / Licensing Standards**						

Course Objectives / Course Learning Rationales (CLRs)

1. Developing Research Skills
2. Understanding Intellectual Property Rights (IPR)
3. Enhancing Ethical Research Practices
4. Promoting Effective Communication of Research Results

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Understand research problem formulation	2	80%	75%
Outcome 2	Analyse research-related information and understand research ethics	2	70%	65%
Outcome 3	Understanding that when IPR would take such an important place in the growth of individuals & nations.	3	80%	70%
Outcome 4	Understand that IPR protection provides an incentive to inventors for further research work and investment in R&D.	3	70%	65%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	2	1	2	2				1		3	2	2	3
Outcome 2	3	2	3	3				2		3	3	2	3
Outcome 3	3	3	3	2				1		3	2	2	3
Outcome 4	3	2	3	2				2		3	3	3	3
Average	3	2	3	2				2		3	3	2	3

Course Unitization Plan

Session	Description of Topic	Contact hours	CLOs Addressed	Reference
1	**Unit I**	**6**		
2	Meaning of research problem, Sources of research problem	2	1	1,3
3	Criteria Characteristics of a good research problem,	2	1	1,2,3
4	Errors in selecting a research problem, scope, and objectives of research problem.	2	1	1,2,3
5	**Unit II**	**6**		
6	Approaches of investigation of solutions for research problem, data collection,	2	1,2	1,2,3
7	Analysis, interpretation, Necessary instrumentations.	2	1,2	1,2,3
8	Effective literature studies approaches, analysis Plagiarism, Research ethics.	2	1,2	1,2,3
9	**Unit III**	**6**		
10	Effective technical writing,	2	1,2	1,2
11	how to write report, Paper Developing a Research Proposal,	2	1,2	1,2
12	Format of research proposal, a presentation and assessment by a review committee.	2	1,2	1,2
13	**Unit IV**	**6**		
14	Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research,	2	1,2	1,2,3
15	innovation, patenting, development. International Scenario: International cooperation on Intellectual Property.	2	1,2	1,2,3
16	Procedure for grants of patents, Patenting under PCT.\	1	1,2	1,2,3
17	Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.	1	1,2	1,2,3
18	**Unit V**	**6**		
19	New Developments in IPR: Administration of Patent System.	2	3,4	4,5
20	New developments in IPR; IPR of Biological Systems,	2	3,4	4,5
21	Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.	2	3,4	4,5
22				
	Total Contact Hours	**30**		

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)				End Semester Exam (50%)
		CLA-1 (10%)	Mid-1 (15%)	CLA-2 (10%)	Mid-2 (15%)	
		Th	Th	Th	Th	Th
Level 1	Remember	40%	50%	30%	20%	30%
	Understand					
Level 2	Apply	60%	50%	70%	80%	70%
	Analyse					
Level 3	Evaluate					
	Create					
Total		**100%**	**100%**	**100%**	**100%**	**100%**

Recommended Resources

1. Stuart Melville and Wayne Goddard, “Research methodology: an introduction for science & engineering students’ “Wayne Goddard and Stuart Melville, “Research Methodology: An Introduction”
2. Ranjit Kumar, 2nd Edition, “Research Methodology: A Step-by-Step Guide for beginners” Halbert, “Resisting Intellectual Property”, Taylor & Francis Ltd ,2007.
3. Mayall, “Industrial Design”, McGraw Hill, 1992.
4. Niebel, “Product Design”, McGraw Hill, 1974.
5. Asimov, “Introduction to Design”, Prentice Hall, 1962.

Other Resources

1. Enter Data

Course Designers

1. Dr. Manjesh Kumar, Department of Mechanical Engineering, SRM University-AP, Andhra Pradesh.
2. Dr. Manas Das, Department of Mechanical Engineering, IIT Guwahati

SRM University *AP*, Andhra Pradesh
Neerukonda, Mangalagiri Mandal,
Guntur District, Mangalagiri, Andhra Pradesh – 522240.

Project Part-1

Course Code	VLS 539	**Course Category**	RDIP	**L**	**T**	**P**	**C**
				0	0	12	12
Pre-Requisite Course(s)		**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	ECE	**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. To learn how to define the research objective.
2. To acquire skills to solve the problem statement.
3. To learn how to prepare scientific presentations.
4. To develop skills for project management and writing scientific reports.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Formulate research objective	2	80%	80%
Outcome 2	Describe the method (experiments or simulation to attain objective)	2	65%	60%
Outcome 3	Describe the research outcome through presentation	3	65%	60%
Outcome 4	Learn how to write thesis	2	60%	65%
Outcome 5	Gain knowledge on various instrumentation techniques used during presentations.	3	80%	75%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	2	2		2	1			3	3	3	1	2	2
Outcome 2	2	2		2	1			3	3	3	2	2	1
Outcome 3	2	2		2	1			3	3	3	2	2	1
Outcome 4	2	2		2	1			3	3	3	2	2	2
Outcome 5	2	2		2	3		3	3	3	3	2	3	2
Average	2	2		2	1		3	3	3	3	2	2	2

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit-I	**Definition of Problem**			
	Clearly articulating the problem that the project aims to solve, Describing the current state of affairs and why a solution is necessary	72	1	1,5
Unit-II	**Method**			
	Application of various methods and approaches to ensure successful execution of Project	74	2	1,5
Unit-III	**Description of results**			
	The obtained results must be interpreted utilising appropriate software, tools, and techniques. Validation of results with standard data base	74	3	2,3,5
Unit-IV	**Poster Presentation**			
	Making a scientific presentation of the results obtained with appropriate reasoning.	72	3	2,3
Unit-V	**Writing of manuscript /thesis**			
	Obtained results is summarized in the form thesis/manuscript/report	68	4	4,5
Total Contact Hours		**360**		

Learning Assessment

Bloom's Level of Cognitive Task		**Continuous Learning Assessments (50%)**		**End Semester Exam (50%)**
		Project Review 1 (25%)	**Project Review 2 (25%)**	
Level 1	Remember			
	Understand			
Level 2	Apply	50%	50%	50%
	Analyse			
Level 3	Evaluate	50%	50%	50%
	Create			
Total		**100%**	**100%**	**100%**

Recommended Resources

1. Problem Solving for Engineers and Scientists: A Creative Approach (https://doi.org/10.1007/978-1-4615-3906-3)
2. Matt Carter Designing Science Presentations: A Visual Guide to Figures, Papers, Slides, Posters, and More (ISBN: 0123859697)
3. Garr Reynolds Presentation Zen: Simple Ideas on Presentation Design and Delivery (ISBN: 0321811984)
4. Article, how to write consistently boring scientific literature by Kaj Sand-Jensen. doi/10.1111/j.0030-1299.2007. 15674.x
5. Keshav S. How to read a paper. ACM SIGCOMM Computer Communication Review. 2007 Jul

Other Resources

1.

Course Designers

1. Dr. M. Durga Prakash, Assistant Professor, Department of Electronics and Communication Engineering, SRM university AP.

SRM University *AP*, Andhra Pradesh
Neerukonda, Mangalagiri Mandal,
Guntur District, Mangalagiri, Andhra Pradesh – 522240.

Dissertation Project Final

Course Code	VLS 549	**Course Category**	RDIP	**L**	**T**	**P**	**C**
				0	0	15	15
Pre-Requisite Course(s)	VLS 539	**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	ECE	**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. To introduce innovative ideas or technologies that can enhance the performance, reliability and efficiency of VLSI circuits.
2. To design, develop and implement innovative solutions related to VLSI systems.
3. To learn scientific presentation preparation skills.
4. To develop project management and scientific report writing skills.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Acquire the skills to explore and introduce innovative ideas or technologies to fill the critical research gap in VLSI.	4	70%	70%
Outcome 2	Design, develop and implement explored innovative ideas related to VLSI Systems.	6	80%	75%
Outcome 3	Learn scientific presentation preparation skills	3	80%	80%
Outcome 4	Develop project management and scientific report writing skills	5	85%	80%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	3	3	3			2	3	3	3	3	3	2
Outcome 2	3	3	2	3			2	3	3	3	3	3	2
Outcome 3	2	2	1	2			2	2	3	3	1	2	3
Outcome 4	2	2	1	2			2	2	3	3	1	2	3
Average	3	3	2	3			2	3	3	3	2	3	3

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit-I	**Definition of Problem & Methodology**			
	Clearly articulating the problem that the project aims to solve, Describing the current state of affairs and why a solution is necessary. Articulating the application of various methods and approaches to ensure the successful execution of the Project.	50	1	1,5
Unit-II	**Design & Implementation**			
	Design and implementation of as-formulated innovative ideas, Critical analysis of results, and evaluate the performance of the VLSI system.	100	2	1,5
Unit-III	**Description & Validation of results**			
	The obtained results must be interpreted utilizing appropriate software, tools, and techniques. Validation of results with standard database.	50	2	2,3,5
Unit-IV	**Scientific Presentation**			
	Making a scientific presentation of the results obtained with appropriate reasoning.	70	3	2,3,4
Unit-V	**Manuscript & Thesis Writeup**			
	Obtained results are summarized in the form Thesis/Manuscript/Report.	80	4	2,4,5
Total Contact Hours		**350**		

Learning Assessment

Bloom's Level of Cognitive Task		**Continuous Learning Assessments (50%)**		**End Semester Exam (50%)**
		Project Review 1 (25%)	**Project Review 2 (25%)**	
Level 1	Remember			
	Understand			
Level 2	Apply	50%	50%	50%
	Analyse			
Level 3	Evaluate	50%	50%	50%
	Create			
Total		**100%**	**100%**	**100%**

Recommended Resources

1. Problem Solving for Engineers and Scientists: A Creative Approach (https://doi.org/10.1007/978-1-4615-3906-3)
2. Matt Carter Designing Science Presentations: A Visual Guide to Figures, Papers, Slides, Posters, and More (ISBN: 0123859697)
3. Garr Reynolds Presentation Zen: Simple Ideas on Presentation Design and Delivery (ISBN: 0321811984)
4. Article, how to write consistently boring scientific literature by Kaj Sand-Jensen. doi/10.1111/j.0030-1299.2007. 15674.x
5. Keshav S. How to read a paper. ACM SIGCOMM Computer Communication Review. 2007 Jul 20;37(3):83-4.

Other Resources

1.

Course Designers

1. Dr. Patta Supraja. Asst. Professor. Dept. Of ECE. SRM University – AP
2. Dr. M. Durga Prakash. Asst. Professor. Dept. Of ECE. SRM University – AP

SRM University *AP*, Andhra Pradesh
Neerukonda, Mangalagiri Mandal,
Guntur District, Mangalagiri, Andhra Pradesh – 522240.

Semiconductor Device Modelling

Course Code	VLS 533	Course Category	Technical Elective	L	T	P	C
				3	1	0	4
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)			
Course Offering Department	ECE	Professional / Licensing Standards					

Course Objectives / Course Learning Rationales (CLRs)

1. Learn the basics of current flow though solid state semiconductor devices.
2. Understand some elementary concepts of quantum- and statistical-mechanics.
3. Gain knowledge of electrostatics of P-N junction diodes.
4. Learn the design of Bipolar transistors.
5. Understand the design of MOSFETs
6. Apply theoretical knowledge of performance of BJTs and MOSFETs using ABACUS simulation tool.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Identify current flow though semiconductor devices	2	70%	65%
Outcome 2	Identify concepts of quantum- and statistical-mechanics	2	70%	65%
Outcome 3	Discuss electrostatics of P-N junction diodes	3	70%	65%
Outcome 4	Discuss BJT and MOSFET design	3	70%	65%
Outcome 5	Illustrate the applications of MOSFETs design	4	70%	65%
Outcome 6	Demonstrate BJTs and MOSFETs design using ABACUS	4	70%	65%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	1	1	2	2	3	2	2	2	3	2	2	1	2
Outcome 2	1	2	2	2	1	2	2	3	3	3	2	1	2
Outcome 3	1	2	2	2	1	2	2	3	2	3	2	1	2
Outcome 4	1	2	2	2	3	3	3	3	3	3	3	1	2
Outcome 5	2	2	3									2	3
Outcome 6	2	2	2									2	2
Average	2	1	2	2	2	2	2	3	3	3	2	2	2

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit I	**Basic Semiconductor Properties & Elements of Quantum Mechanics**	**9**		
1.	General Material Properties	2	1	1,3
2.	Crystal Structure, The Unit Cell Concept	1	1	1,3
3.	Simple 3-D Unit Cells	1	2	1,3
4.	Bravais Lattices and Crystal Systems	1	3	1,3
5.	Specific Semiconductor Lattices	1	2	1,3
6.	Miller Indices, Example Use of Miller Indices	1	2	1,3
7.	The Quantum Concept	1	2	1,3
8.	Basic Formalism, Simple Problem Solutions	1	2	1,3
Unit II	**Energy Band Theory & Equilibrium Carrier Statistics**	**9**		
9.	Preliminary Considerations, Approximate One-Dimensional Analysis	2	1	1,4
10.	Extrapolation of Concepts to Three Dimensions	2	1	1,4
11.	Density of States, Fermi Function	1	2	1,4
12.	Equilibrium Distribution of Carriers	1	3	1,4
13.	The Energy Band Diagram, Donors	1	2	1,4
14.	Acceptors, Band Gap Centers	1	2	1,4
15)	Equilibrium Concentration Relationships, Concentration and E_F Calculations.	1	2	1,4
Unit III	**Recombination-Generation Processes & Carrier Transport**	**9**		
16.	Introduction	1	2	2,3
17.	Recombination-Generation Statistics	2	2	2,3
18.	Surface Recombination-Generation	2	2	2,3
19.	Supplemental R-G Information	1	2	2,3
20.	Drift	1	2	2,3
21.	Diffusion	1	2	2,3
22.	Equations of State	1	2	2,3
Unit IV	**Electrostatics of P-N Junction Diodes & Introduction to Bipolar Transistors**	**9**		
23.	P-N Diode I-V Characteristics	1	3	2,4
24.	Non-ideal Effects	1	3	2,4
25.	AC Response	1	3	2,4
26.	Large Signal Response	1	4	2,4
27.	Schottky Diode I	1	4	2,4
28.	Schottky Diode II	1	3	2,4
29.	BJT Design I	1	4,5,6	2,4
30.	BJT Design II	1	4,5,6	2,4
31.	Heterojunction Bipolar Transistors	1	4,5,6	2,4
Unit V	**MOS**	**9**		
32.	MOS Electrostatics	2	4	2,4
33.	MOSCAP Frequency Response	1	4	2,4
34.	MOSFET I-V Characteristics	2	4	2,4
35.	Nonideal Effects in MOSFET	2	4	2,4
36.	Modern MOSFET	1	3	2,4
37.	Reliability of MOSFET	1	3	2,4
Total Contact Hours		**45**		

Course Unitization Plan - Tutorials

Session No.	Description of Experiments	Required Contact Hours	CLOs Addressed	References Used
1.	Interactive visualization of different Bravais lattices, and crystal planes, and materials (diamond, Si, InAs, GaAs, graphene, buckyball).	2	2	4,5
2.	Study of Band Models / Band Structure	2	3	4,5
3.	Carrier Distributions: demonstrates electron and hole density distributions based on the Fermi-Dirac and Maxwell Boltzmann equations	2	3,5,6	4
4.	Understand the basic concepts of DRIFT and DIFFUSION of carriers inside bulk semiconductors	2	3,5,6	4
5.	Simulate semiconductor process modeling	2	3,5,6	4
6.	Basic concept of PN Junction devices	2	3	4,5
7.	Study of Solar Cells	2	3	5
8.	Simulate npn and pnp Bipolar Junction Transistors (BJTs)	2	4	4,5
9.	Analysis of MOS Capacitors	2	4	4
10.	Implement MOSFET / Many-Acronym-Device-FET (mad-FETs)	4	4	4,5
Total Contact Hours		**22**		

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)					End Semester Exam (50%)	
		Theory (30%)				Tutorial/Practical (20%)		
		CLA-1 (5%)	Mid-1 (10%)	CLA-2 (5%)	CLA-3 (10%)		Th	Tut/Prac
Level 1	Remember	60%	40%	60%		50%	30%	40%
	Understand							
Level 2	Apply	40%	60%	40%	70%	50%	60%	60%
	Analyse							
Level 3	Evaluate				30%		10%	
	Create							
Total		**100%**	**100%**	**100%**	**100%**	**100%**	**100%**	**100%**

Recommended Resources

1. Advanced Semiconductor Fundamentals, Second Edition, by Robert F. Pierret, Pearson Education, Inc. (1983).
2. Semiconductor Device Fundamentals, Robert F.Perret, (1996).
3. Sze, S. M., & Ng, K. K. (2006). Physics of semiconductor devices. John wiley& sons.
4. B. G. Streetman, S. K. Banerjee, Solid State Electronic Devices, Pearson, (2016)
5. Arora, N. (2007). MOSFET modeling for VLSI simulation: theory and practice. World Scientific.

Other Resources

1. https://nptel.ac.in/courses/117106033
2. https://onlinecourses.nptel.ac.in/noc23_ee35/preview

Course Designers

1. Dr. M. Durga Prakash, Assistant Professor, Department of ECE, SRM University – AP

SRM University *AP*, Andhra Pradesh
Neerukonda, Mangalagiri Mandal,
Guntur District, Mangalagiri, Andhra Pradesh – 522240.

Hardware Accelerators for IoT Edge Computing

Course Code	VLS 535	**Course Category**	Technical Elective	**L**	**T**	**P**	**C**
				3	1	0	4
Pre-Requisite Course(s)		**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	ECE	**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. To understand DNN structures, Opportunities and Challenges with custom HW Accelerators and recent developments in DNN hardware/Chip Designs from various leading companies
2. To understand how DNN computations are mapped to various hardware platforms and understand the tradeoffs between various architectures/platforms and being able to evaluate different DNN accelerator implementations with benchmarks and performance comparison metrics
3. To get familiar with emerging techniques for processing DNNs on edge devices such as Approximate Computing for DNNs, Precision scalable architectures and emerging NVMs for DNNs.
4. To understand and get hands on implementing various DNN architectures on hardware like CPU, GPU, FPGA, ASIC, etc.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Clearly understand what are DNNs, models, datasets and architectures	2	70%	65%
Outcome 2	evaluate the key design considerations for efficient DNN processing and understand tradeoffs between various hardware architectures and platforms	3	70%	65%
Outcome 3	Understand and implement emerging techniques for processing DNNs on edge devices such as Approximate Computing for DNNs, Precision scalable architectures and emerging NVMs for DNNs, CiM	3	70%	65%
Outcome 4	Implement various models on hardware platforms	3	70%	65%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	3	3	2	1		2					3	3
Outcome 2	3	3	3	2	2	1	2		3			2	3
Outcome 3	3	3	3	2	2		2		3			3	3
Outcome 4	3	3	3	3	2	1	2		3			2	3
Average	3	3	3	2	2	1	2		2			2	3

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit 1	**Introduction to Hardware accelerators, IoT Edge Computing, DNNs and Applications**	**8**		
1.	Overview of ML/Deep Learning and Applications,	2	1	1,2,3
2.	Training vs Inference, IoT Embedded vs Cloud Computing	2	1	1
3.	Overview of DNN Components, DNN layers, Popular types of Deep Neural Networks-FN,CNNs, RNNs, LSTM,	2	1	1
4.	Light weight NN Models	2	1	1,2
Unit 2	**DNN models**	**10**		
6.	Popular DNN models	2	1,2	1
7.	HW-SW Co-Design	2	1,2	1
8.	CNNs and implementation	3	1,2	1
9.	DNN development resources	3	1,2	1
Unit 3	**DNN key metrics, Design objectives, hardware platforms**	**10**		
10.	Accuracy, Throughput, Latency	2	2,3,4	1
11.	Power, energy, flexibility, scalability	3	2,3,4	1
12.	Designing DNN accelerators	2	2,3,4	1
13.	Accelerating DNNs in Hardware: study and analysis of various recent platforms on CPU, GPU, FPGA, ASIC platforms	3	2,3,4	1
14.	Architectures of Google's TPU, Apple's Neural Engine, ARM's Project Trillium, etc	2	2,3,4	1
Unit 4	Review of Python & Verilog for FPGA, CAD Tools for ASIC implementations	**10**		
15.	Review of Python for DNNs with examples	4	2,3,4	1
16.	Review and design of DNNs with HDLs	3	2,3,4	1
17.	Review of cadence EDA based system design for DNNs	3	2,3,4	1
Unit 5	Emerging Techniques for DNN processing on edge devices	**8**		
18.	Precision scalable architectures	2	3	1
19.	Approximate Computing techniques	2	3	1
20.	In-memory computing architectures	2	3	1
21.	Emerging NVMs for DNN processing	2	3	1
	Total	**46**		

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (60%)								End Semester Exam (40%)	
		CLA-1 (15%)		Mid (15%)		CLA-2 (15%)		CLA-3 (15%)			
Level 1	Remember	60%		50%		60%		50%		40%	
	Understand										
Level 2	Apply	40%		50%		40%		50%		60%	
	Analyze										
Level 3	Evaluate										
	Create										
Total		**100%**		**100%**		**100%**		**100%**		**100%**	

Recommended Resources

1. Vivienne Sze , Yu-Hsin Chen , Tien-Ju Yang, Joel S. Emer, Efficient Processing of Deep Neural Networks, Springer, 2020. https://link.springer.com/book/10.1007/978-3-031-01766-7
2. Deep Learning by Ian Goodfellow and Yoshua Bengio and Aaron Courville, MIT Press, https://www.deeplearningbook.org/
3. Neural Networks and Deep Learning, http://neuralnetworksanddeeplearning.com/

Other Resources

1.

Course Designers

1. Dr. Ramesh Vaddi, Associate Professor, Dept of ECE, SRM University - AP

SRM University *AP*, Andhra Pradesh
Neerukonda, Mangalagiri Mandal,
Guntur District, Mangalagiri, Andhra Pradesh – 522240.

Sensor Technology and MEMS

Course Code	VLS 562	**Course Category**	Technical Elective	**L**	**T**	**P**	**C**
				3	1	0	4
Pre-Requisite Course(s)	VLS 513	**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	ECE	**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. To understand MEMS and microfabrication
2. To study the essential material properties.
3. To study various sensing and transduction technique.
4. To know various fabrication and machining process of MEMS
5. To know about the polymer and optical MEMS

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Be familiar with the important concepts applicable to MEMS and their fabrication	2	70%	65%
Outcome 2	Discuss the design, analysis and testing of MEMS required material properties	2	70%	65%
Outcome 3	Discuss the various sensing and transduction techniques	3	70%	65%
Outcome 4	Discuss various fabrication and machining process of MEMS	3	70%	65%
Outcome 5	Illustrate the applications of the polymer and optical MEMS devices	4	70%	65%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	1	1	2	2	3	2	2	2	3	2	2	1	2
Outcome 2	1	2	2	2	1	2	2	3	3	3	2	1	2
Outcome 3	1	2	2	2	1	2	2	3	2	3	2	1	2
Outcome 4	1	2	2	2	3	3	3	3	3	3	3	1	2
Outcome 5	2	2	3									2	3
Outcome 6	2	2	2									2	2

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit I	**Introduction to Microfabrication**	**10**		
1	Review of Photolithography	2	1	1,3
2	Thin Film Deposition, Thermal Oxidation of Silicon	2	1	1,3
3	Wet Etching, Silicon Anisotropic Etching, Plasma Etching and Reactive Ion Etching	2	2	1,3
4	Doping	1	3	1,3
5	Wafer Dicing, Wafer Bonding	1	2	1,3
6	Packaging and Integration	1	2	1,3
7	Surface Micromachining	1	2	1,3
Unit II	**Electrical and Mechanical Concepts**	10		
8	Conductivity of Semiconductor	1	1	1,2
9	Crystal Planes and Orientations	2	1	1,2
10	Stress and Strain	1	2	1,2
11	Flexural Beam Bending Analysis Under Simple Loading Conditions	2	3	1,2
12	Intrinsic Stress, Dynamic System	2	2	1,2
13	Resonant Frequency, and Quality Factor	2	2	1,2
Unit III	**Electrostatic and Thermal Sensing and Actuation**	**8**		
16.	Parallel-Plate Capacitor, Applications of Parallel-Plate Capacitors (Inertia Sensor, Pressure Sensor, Flow Sensor, Tactile Sensor, Parallel-Plate Actuators)	2	2	2,3
17.	Interdigitated Finger Capacitors, Applications of Comb-Drive Device (Inertia Sensors, Actuators)	2	2	2,3
18.	Thermal Sensors and Actuators, Fundamentals of Thermal Transfer, Sensors and Actuators Based on Thermal Expansion	2	2	2,3
19.	Thermocouple and Thermal resistors, Applications (Inertia Sensors, Flow sensors, Infrared sensors)	2	2	2,3
Unit IV	**Piezoresistive Sensors and Piezoelectric Sensing and Actuation**	**9**		
23.	Expression of Piezoresistivity, Piezoresistive Sensor Material (Single Crystal Silicon, Polycrystalline Silicon)	2	3	1,2
24.	Stress Analysis of Mechanical Elements, Applications of Piezoresistive Sensors (Inertia Sensor, Pressure Sensor, Flow Sensor, Tactile Sensor);	4	3	1,2
25.	Mathematical Description of Piezoelectric Effects, Properties of Piezoelectric Materials, Applications (Inertia Sensor, Acoustic, Flow Sensor, Tactile Sensor).	4	3	1,2
Unit V	**Polymer MEMS, Microfluidics and Case Studies**	**8**		
32.	Polymers in MEMS, Applications of polymers	2	4	2,3
33.	Fluid Mechanics Concepts, Microfluidic channels and valves	2	4	2,3
34.	Case studies (Capacitive accelerometer, Piezoelectric Gyroscope)	2	4	2,3
35.	Case studies (DNA amplification, Microbridge gas sensor)	2	4	2,3
Total Contact Hours		**45**		

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)				End Semester Exam (50%)
		Theory (30%)				
		CLA-1 (5%)	Mid-1 (10%)	CLA-2 (5%)	Mid-2 (10%)	Th
Level 1	Remember	60%	40%	60%	40%	30%
	Understand					
Level 2	Apply	40%	60%	40%	60%	70%
	Analyse					
Level 3	Evaluate					
	Create					
Total		**100%**	**100%**	**100%**	**100%**	**100%**

Recommended Resources

1. S.M.Sze, "VLSI Technology", McGraw Hill, 2nd Edition. 2008
2. Chang Liu, "Foundations of MEMS" Prentice Hall, 2012
3. 3.S D Senturia, "MICROSYSTEM DESIGN", Kluwer Academic Publishers, 2002

Other Resources

1.

Course Designers

1. Dr. M. Durga Prakash, Assistant Professor, Department of ECE, SRM University – AP

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Guntur District, Mangalagiri, Andhra Pradesh – 522240.

CAD for VLSI

Course Code	VLS 530	**Course Category**	Technical Elective	**L**	**T**	**P**	**C**
				3	0	1	4
Pre-Requisite Course(s)		**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	ECE	**Professional / Licensing Standards**	IEEE, Microsoft, Cadence, Vivado				

Course Objectives / Course Learning Rationales (CLRs)

1. To study the various CAD tools and methodologies employed in the design of VLSI circuits.
2. To understand the RTL (Register-Transfer Level) design, logic synthesis, physical design, and simulation.
3. To learn design and testing of VLSI circuits using CAD tools.
4. To evaluate and enhance the performance of VLSI designs through CAD tools.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Learn industry-standard CAD tools, navigating schematic capture, layout design, and verification tools for VLSI circuits.	2	80%	70%
Outcome 2	Apply theoretical concepts into practical applications.	3	70%	60%
Outcome 3	Analyse, identify bottlenecks, optimize VLSI designs for Performance, Power, and Area (PPA) using CAD tools.	4	80%	70%
Outcome 4	Exhibit adaptability to evolving CAD technologies, ensuring they stay current with advancements in the dynamic field of VLSI design.	4	70%	60%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	1	2					2				1	2
Outcome 2	3	2	3					3			1	3	2
Outcome 3	3	3	3					2			1	3	3
Outcome 4	3	3	3					3			1	3	3
Average	3	3	3					3			1	3	3

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOsAddressed	References
Unit 1	**Introduction to VLSI Design and CAD Tools**	**9**		
	Understand the stages of the VLSI design process, from conceptualization to fabrication.	1	1	1,2
	Trace the historical development of VLSI technology and its impact on computing.	1	1	1,2
	Examine key milestones and breakthroughs that shaped the VLSI landscape.	1	1	1,2
	Analyze the pivotal role of Computer-Aided Design (CAD) tools in VLSI design.	1	1,2	1,2
	Discuss how CAD tools enhance efficiency, accuracy, and productivity in VLSI workflows.	1	1,2	1,2
	Explore Electronic Design Automation (EDA) tools and their roles in the design flow.	1	1,2	1,2
	Discuss the impact of CAD tools on reducing time-to-market and overall design cost.	1	1,2	1,2
	Introduce students to a basic CAD tool interface.	1	1,2	1,2,4,6
	Conduct introductory exercises to familiarize students with basic CAD operations.	1	1,2	1,2,4,6
Unit 2	**Digital Design Fundamentals**	**9**		
	Apply Boolean algebra to simplify and manipulate logical expressions.	1	2,3	1,2
	Design and analyze combinational circuits using logic gates.	1	2,3	1,2
	Introduce sequential circuits, including flip-flops and latches.	1	1,2,3	1,2
	Discuss the concept of clocking and its importance in sequential circuit design.	1	1,2,3	1,2
	Define Register-Transfer Level (RTL) design and its role in VLSI.	1	1,2,3	1,2
	Demonstrate the translation of high-level design concepts into RTL descriptions.	1	1,2,3	1,2
	Engage students in practical RTL design exercises.	1	2,3	1,2
	Implement simple digital circuits using RTL design principles.	1	2,3	1,2
	Utilize simulation tools to validate the functionality of RTL designs.	1	2,3	1,2
Unit 3	**Schematic Capture and Simulation Tools**	**9**		
	Introduce functional simulation using Verilog or VHDL.	1	2,3,4	1,2,3
	Create and simulate basic digital circuits to understand functional behavior.	1	2,3,4	1,2,3
	Optimize circuit designs for better performance using timing constraints	1	2,3,4	1,2,3
	Apply simulation tools to analyze and troubleshoot real-world digital circuits.	1	2,3,4	1,2,3
	Discuss the significance of simulation in identifying design flaws.	1	2,3,4	1,2,3
	Introduce advanced simulation techniques such as mixed-signal simulation.	1	2,3	1,2,3
	Explore co-simulation of analog and digital components.	1	2,3,4	1,2,3
	Conduct hands-on sessions for students to create and simulate circuits using schematic capture tools.	1	2,3,4	1,2,3

	Emphasize the practical application of simulation results in design refinement.	1	2,3	1,2,3
Unit 4	**Logic Synthesis and Optimization Techniques**	**9**		
	Define logic synthesis and its role in transforming RTL descriptions into gate-level netlists.	1	2,3,4	1,2,5
	Discuss strategies for optimizing designs in terms of area, power, and performance (PPA).	1	2,3,4	1,2,5
	Introduce technology mapping as a critical step in the synthesis process.	1	2,3,4	1,2,5
	Cover advanced logic synthesis techniques, including retiming and resynthesis.	1	2,3,4	1,2,5
	Explore the impact of these techniques on design quality and efficiency.	1	2,3,4	1,2,5
	Demonstrate the application of logic synthesis techniques through practical examples.	1	2,3,4	1,2,5
	Guide students in optimizing designs for specific criteria.	1	2,3,4	1,2,5
	Discuss current challenges in logic synthesis.	1	2,3,4	1,2,5
	Explore emerging trends and future directions in logic synthesis research and development.	1	2,3,4	1,2,5
Unit 5	**Physical Design and Layout**	**9**		
	Provide an overview of the physical design process, from initial floor planning to tape-out.	1	3,4,5	1,2,5
	Introduce floor planning as a critical step in physical design.	1	2,3,4	1,2,5
	Explain the global and detailed routing stages in the physical design flow.	1	2,3,4	1,2,5
	Discuss algorithms and techniques for efficient and effective routing.	1	3,4,5	1,2,5
	Cover the significance of physical verification in ensuring design correctness.	1	2,3,4	1,2,5
	Introduce Design Rule Checking (DRC) and its role in identifying layout violations.	1	2,3,4	1,2,5
	Conduct hands-on sessions for students to implement physical design principles.	1	3,4,5	1,2,5
	Guide students through the process of floorplanning, placement, and routing.	1	2,3,4	1,2,5
	Discuss advanced topics such as clock tree synthesis and power planning.	1	2,3,4	1,2,5
	Total			**45**

Learning Assessment

Bloom's Level of Cognitive Task		**Continuous Learning Assessments (50%)**				**End Semester Exam (50%)**
		CLA-1 (10%)	**Mid-1 (15%)**	**CLA-2 (10%)**	**Mid-2 (15%)**	
Level 1	Remember	80%	50%	20%	20%	20%
	Understand					
Level 2	Apply	20%	50%	80%	80%	80%
	Analyse					
Level 3	Evaluate					
	Create					
Total		**100%**	**100%**	**100%**	**100%**	**100%**

More Than Moore's Electronics

Course Code	VLS 555	**Course Category**	Departmental Core Elective	**L**	**T**	**P**	**C**
				3	1	0	4
Pre-Requisite Course(s)	VLSI Technology	**Co-Requisite Course(s)**		**Progressive Course(s)**			
Course Offering Department	ECE	**Professional / Licensing Standards**					

Course Objectives / Course Learning Rationales (CLRs)

1. To explore the limitations and challenges associated with traditional Moore's Law scaling and delve into alternative approaches for improving electronic devices.
2. To study and analyze emerging technologies that contribute to electronic advancements, such as 3D integration, heterogeneous integration, and new materials.
3. To gain proficiency in designing electronic systems with an emphasis on energy efficiency, thermal management, and overall system efficiency by taking into account power optimization.
4. Recognize the interdisciplinary nature of More than Moore's Electronics by exploring contributions from fields such as materials science, physics, and engineering.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Understand the limitations and challenges associated with traditional Moore's Law scaling and delve into alternative approaches for improving electronic devices	3	80%	75%
Outcome 2	Understand and analyze the emerging technologies that contribute to electronic advancements, such as 3D integration, heterogeneous integration, and new materials	4	85%	80%
Outcome 3	Design electronic systems with an emphasis on energy efficiency, thermal management, and overall system efficiency	6	80%	75%
Outcome 4	Understand the interdisciplinary nature of More than Moore's Electronics and strongly motivated towards integration of materials science, physics, and engineering research into designing future 3D-IC systems.	5	85%	75%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tools and ICT Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	2	2	3	2	2	2	3	3	3	2	1	2	3
Outcome 2	3	2	3	2	1	2	2	2	3	3	2	3	3
Outcome 3	3	2	3	2	1	2	3	2	3	3	3	3	3
Outcome 4	3	2	2	2	3	2	3	2	3	3	3	3	2

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
UNIT I	**Introduction to 3D-IC technology**	**14**		
	Introduction to Moore's Law and MOSFET Technology	2	1	1,2,3
	Scaling Theory	2	1	1,2,3
	Evolution of MOSFET	5	1	1,2,3
	Requirements to go beyond Moore's Law	2	1	1,2,3
	Transistor scaling & Research roadmap	2	1	1,2,3
	CMOS feature directions	1	1	1,2,3
Unit II	**3D-Interconnects**	**6**		
	Classification and advantages of 3-D Integration	1	2,4	1,2,3
	Interconnects scaling theory and performance evolution,	2	2,4	1,2,3
	3D Interconnects	1	2,4	1,2,3
	On-chip device (vs) Interconnected device	1	2,4	1,2,3
	3D device (vs) Multicore device.	1	2,4	1,2,3
Unit III	**3D-Bonding**	**16**	2,4	
	Interconnect Technology & Classification of Interconnects	1	2,4	1,2,3
	Blanket and Non-Blanket bonding	2	2,4	1,2,3
	Direct bonding and Thermo-Compression bonding	3	2,4	1,2,3
	Passivated and Un-passivated bonding	2	2,4	1,2,3
	Metallic, Dielectric and Hybrid bonding	2	2,4	1,2,3
	Bond quality characterization techniques	2	2,4	1,2,3
	Grand challenges in bonding technology	1	2,4	1,2,3
	Wafer orientation strategies in 3D stacks	2	2,4	1,2,3
	Daisy Chain	1	2,4	1,2,3
UNIT IV	**Through-Silicon-Via (TSV)**	**6**		
	TSV Classification and Fabrication methods	1	3,4	1,2,3
	TSV Integration strategies	1	3,4	1,2,3
	TSV Cooling strategies	1	3,4	1,2,3
	TSV Electrical & Thermal modelling	2	3,4	1,2,3
	TSV Testing	1	3,4	1,2,3
UNIT V	**Other Si Electronics**	**7**		
	Spintronics, Spin FET	2	4	4
	Magnetic Tunnel Junction, Spin Transistors	2	4	4
	Organic Electronics, Organic Light Emitting Diodes (OLED), Organic Thin Film Transistors (OTFT)	2	4	4
	Organic Photovoltaic Cells (OPC)	1	4	4
Total Contact Hours		**49**		

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (60%)				End Semester Exam (40%)
		CLA-1 (15%)	Mid-1 (15%)	CLA-2 (15%)	CLA-3 (15%)	
Level 1	Remember	50%	45%	30%	50%	40%
	Understand					
Level 2	Apply	40%	50%	50%	40%	50%
	Analyse					
Level 3	Evaluate	10%	5%	20%	10%	10%
	Create					
Total		**100%**	**100%**	**100%**	**100%**	**100%**

Recommended Resources

1.

Other Resources

1.

Course Designers

1. Dr. Patta Supraja. Asst. Professor. Dept. Of ECE. SRM University – AP With reference to Dr. Shiv Govind Singh, Professor, Dept. Of EE. IIT Hyderabad.