Department of Electronics and Communication Engineering

MTech. VLSI
Curriculum and Syllabus
(Applicable to the students admitted from AY 2023-24 onwards)

School of Engineering and Sciences
SRM University-AP, Andhra Pradesh

M. Tech in VLSI

Vision Statement

To be a globally recognized leader in the field of Electronics and Communications, by fostering innovation through cutting-edge collaborative research to inform interdisciplinary education.

Mission Statements

- Create inclusive and highly motivated individuals and leaders who promote diversity, innovation, creativity, and a high sense of responsibility towards societal progress.
- Strive for excellence by promoting interdisciplinary education and research through global collaborations.
- Deliver state-of-the-art research-based education that equips students with the skills to address contemporary challenges and contribute to the field's advancement.
- Foster a culture of innovation and entrepreneurship, by working closely with leading industry partners to translate ideas into real-life solutions.
- Aim to be a global knowledge hub by collaborating with leading institutions and industries.

Program Educational Objectives (PEOs)

PEO 1: Enable the postgraduate students to learn the fundamentals deeply and lay a strong foundation for their professional careers or higher studies.

PEO 2: Train the students to have hands-on VLSI System design skills which can be applied to solve industrial and research problems in an interdisciplinary environment.

PEO 3: Train the students to have comprehensive knowledge and skills in VLSI technologies which can be applied to the given problems in industrial and research multi-disciplinary environments.

PEO 4: Facilitate the development of effective communication skills, lifelong learning, leadership qualities, and ethical professional conduct across their higher education and career paths.

Mission of the Department to Program Educational Objectives (PEO) Mapping

	PEO 1	PEO 2	PEO 3	PEO 4
Mission Statement 1	3	3	2	2
Mission Statement 2	3	3	2	2
Mission Statement 3	3	2	3	2
Mission Statement 4	3	2	3	3
Mission Statement 5	3	3	3	2

Program Outcomes (PSOs)

PSO-1: Recognize, research, and resolve a wide range of practical issues in the field of VLSI.

PSO-2: Develop skills to build and create systems in the expanding fields of VLSI to solve the problems of the modern economy.

PSO-3: Demonstrate exemplary leadership attributes and actively pursue the advancement of many entities, including organizations, the environment, and society at large by upholding their professional obligations with a strong commitment to ethical conduct.

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tool Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Team work	Communication	Life-long Learning	PSO1	PSO2	PSO3
PEO 1	**3**	**3**	**3**	**3**	**2**	**1**	**3**	**2**	**2**	**2**	**3**	**2**	**2**
PEO 2	**3**	**3**	**3**	**3**	**3**	1	**3**	1	**2**	**2**	**3**	**2**	**3**
PEO 3	**3**	**3**	**3**	**3**	3	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**3**
PEO 4	**2**	**3**	**2**	2	**2**	**3**	**3**	1	2	2	**3**	**3**	3

Programme Outcomes (POs)

PO 1: Engineering Knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO 2: Design / Development of Solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for public health and safety and cultural, societal, and environmental considerations.

PO 3: Conduct Investigations of Complex Problems: Use research-based knowledge and research methods, including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions for complex problems.

PO 4: Modern Tool Usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools, including prediction and modelling, to complex engineering activities with an understanding of the limitations.

PO 5: The Engineer and Society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO 6: Environment and Sustainability: Understand the impact of professional engineering solutions in societal and environmental contexts and demonstrate the knowledge of and need for sustainable development.

PO 7: Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO 8: Individual and Teamwork: Function effectively as an individual and as a member or leader in diverse teams and in multidisciplinary settings.

PO 9: Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO 10: Life-long Learning: Recognize the need for and have the preparation and ability to engage in independent and lifelong learning in the broadest context of technological change.

Category	Semester					
	I	II	III	IV	Total	%
Ability Enhancement Courses - AEC	1	1	0	0	2	2.5
Value Added Courses - VAC	1	1	0	0	2	2.5
Skill Enhancement Courses - SEC	2	2	0	0	4	5
Foundation / Interdisciplinary Courses - FIC	3	0	0	0	3	3.75
CC / SE / CE / TE / DE / HSS	16	16	0	0	32	42.5
Minor / Open Elective - OE	0	0	0	0	0	0
(Research/ Design/ Industrial Practice/Project/Thesis/Internship) -RDIP	0	3	17	15	35	43.75
Grand Total	22	26	17	15	80	100

M. Tech Curriculum in VLSI- 2023

SEMESTER I									
S. No	**Category**	**Sub-Category**	**Course Code**	**Course Title**	**L**	**T/D**	**P/Pr**	**C**	**LH**
1	VAC	AEC	VAC 501	Community Engagement and Social Responsibility	0	0	1	1*	30
2	AEC	AEC	AEC 502	Research Seminar	0	0	1	1	30
3	SEC	SEC	SEC 502	Design Thinking	1	0	1	2	60
4	FIC	FIC	FIC 503	AI/ML Techniques	2	0	1	3	90
5	Core	CC	VLS 501	CMOS Digital IC Design	3	0	1	4	120
6	Core	CC	VLS 502	CMOS Analog and Mixed Signal IC Design	3	0	1	4	120
7	Core	CC	VLS 503	VLSI Technology	3	1	0	4	120
8	Core	CC	VLS 504	VLSI Physical Design	3	0	1	4	120
				Semester Total	**15**	**1**	**7**	**22**	**690**

SEMESTER II									
S. No	**Category**	**Sub-Category**	**Course Code**	**Course Title**	**L**	**T/D**	**P/Pr**	**C**	**LH**
1	VAC	AEC	VAC 502	Community Engagement and Social Responsibility	0	0	1	1*	30
2	AEC	AEC	AEC 503	Research Seminar	0	0	1	1	30
3	SEC	SEC	SEC 103	Entrepreneurial mindset	1	0	1	2	60

4	Elective	CE	CE	Industry - Core Elective	3	0	1	4	120
5	Elective	CE	CE	Industry - Core Elective	3	0	1	4	120
6	Core	CC	VLS 505	VLSI Testing and Verification	3	0	1	4	120
7	Core	CC	VLS 506	Semiconductor Device Modelling	3	0	1	4	120
8	Core	CC	VLS 507	Advanced HDL based FPGA Design	3	0	1	4	120
9	RDIP	RDIP	VLS 508	Project Management	0	2	1	3	90
				Semester Total	**16**	**2**	**9**	**26**	**810**

SEMESTER III									
S.No	**Category**	**Sub-Category**	**Course Code**	**Course Title**	**L**	**T/D**	**P/Pr**	**C**	**LH**
1	RDIP	RDIP	VLS 509	Thesis I	0	0	14	14	420
2	RDIP	RDIP	VLS 510	Industrial Practice	0	0	3	3	90
				Semester Total	**0**	**0**	**17**	**17**	**510**

SEMESTER IV									
S.No	**Category**	**Sub-Category**	**Course Code**	**Course Title**	**L**	**T/D**	**P/Pr**	**C**	**LH**
1	RDIP	RDIP	VLS 511	Thesis II	0	0	15	15	450
				Semester Total	**0**	**0**	**15**	**15**	**450**

Note: L-T/D-P/Pr and the class allocation is as follows.

a. Every 1 credit of Lecture/Tutorial per week is equal to one contact hour of 60 minutes
b. Every 1 credit of Discussion per week is equal to two contact hours of 60 minutes
c. Every 1 credit of Practical per week is equal to two contact hours of 60 minutes
d. Every 1 credit of Project per week is equal to two contact hours of 60 minutes (timetable not required)

S.No	**Semester**	**Credits**
1	I	22
2	II	26
3	III	17
4	IV	15
Total		**80**

List of Core Electives									
S. No	**Category**	**Sub-Category**	**Course Code**	**Course Title**	**L**	**T/D**	**P/Pr**	**C**	**LH**
1	CE	CE	VLS 533	Semiconductor Device Modelling	3	0	1	4	120
2	CE	CE	VLS 535	Signal Processing and Computer vision	3	0	1	4	120
3	CE	CE	VLS 562	Sensor Technology and MEMS	3	0	1	4	120
4	CE	CE	VLS 530	CAD for VLSI	3	0	1	4	120
5	CE	CE	VLS 555	More than Moore's electronics	3	0	1	4	120

SEMESTER I

SRM University – AP, Andhra Pradesh

Neerukonda, Mangalagiri Mandal

Guntur District, Mangalagiri, Andhra Pradesh 522240

Design Thinking

Course Code	**SEC 502**	Course Category	**SEC**	L-T-P-C	**1**	**0**	**1**	**2**
Pre-Requisite Course(s)	**NA**	Co-Requisite Course(s)	**NA**	Progressive Course(s)				
Course Offering Department	**Management**	Professional / Licensing Standards	*NA*					

Course Objectives

1. Familiarize with the principles of Design Thinking
2. Learn to apply the principles of Design Thinking
3. Apply Design Thinking to solve problems.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	**Bloom's Level**	**Expected Proficiency Percentage**	**Expected Attainment Percentage**
Outcome 1	Grasp the Concepts and process of Design Thinking	2	85	90
Outcome 2	Learn the process of Design Thinking	2	85	90
Outcome 3	Solve a problem using Design Thinking Principles	4	75	65

Course Articulation Matrix (CLO) to (PLO)

CLOs	**Program Learning Outcomes (PLO)**													
	Management Knowledge	Analytical Reasoning and	Critical and Reflective	Strategic Thinking and	Modern Tools and ICT Usage	Environment and	Moral, Multicultural	Individual and Teamwork	Communication Skills	Leadership Readiness	Self-Directed and Lifelong	PSO 1	PSO 2	PSO 3
Outcome 1	3										1	3	1	3

Outcome 2	3							3			2	3	2	3
Outcome 3	3	3	3	3				3	3	3	3	3	3	3
Course Average	**3**	**3**	**3**	**3**				**3**	**3**	**3**	**2**	**3**	**2**	**3**

Course Unitization Plan - Theory

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit 1	**Incubation and understanding**			1,2
1.	Understanding of Design Thinking & its Importance	4	1	1,2
2.	Importance of Design Thinking	3	1	1,2
3.	Pillars of Design Thinking	3	1	1,2
Unit 2	**Process – Understanding the Stages of Design Thinking**			1,2
4.	Stage 1- Empathy	2	2	1,2
5.	Stage 2 - Define	2		
6.	Stage 3 – Ideate	2		
7.	Stage 4 – Prototype	2	2	1,2
8.	Stage 5 – Test & Implement	2	2	1,2
Unit 3	**Application**			
9.	Project Work	7	3	1,2
10.	Viva	3	3	1,2
Total Contact Hours		**30**		

Recommended Resources

1. Design Thinking – Techniques and Approaches, N. Siva Prasad

Other Resources

1. HBS – Online – Design Thinking & Innovation – course material
2. Case studies
3. Nigel Cross, Design Thinking, BERG Publishing, (2011)
4. Thomas Lockwood, Design Thinking- Integrating Innovation, Customer Experience and Brand Value, Design Management Institute, (2009)

Learning Assessment (Theory)

Bloom's Level of Cognitive Task		**Continuous Learning Assessments (100%)**	
		CLA-1 (50%)	**CLA-2 (50%)**
Level 1	Remember	20	40
	Understand		
Level 2	Apply	30	30
	Analyse		
Level 3	Evaluate	50	30
	Create		
Total		**100%**	**100%**

Course Designers

a. ***Satyanarayana Duvvuri****, Visiting Faculty, Paari school of business, SRM University AP.*

SRM University – AP, Andhra Pradesh

Neerukonda, Mangalagiri Mandal

Guntur District, Mangalagiri, Andhra Pradesh 522240

AI/ML Techniques

Course Code	**FIC 503**	Course Category	**Core**	L-T-P-C	**2**	**0**	**1**	**3**
Pre-Requisite Course(s)		Co-Requisite Course(s)	**Nil**	Progressive Course(s)	**Nil**			
Course Offering Department	**ECE**	Professional / Licensing Standards						
Board of Studies Approval Date		Academic Council Approval Date						

Course Objectives / Course Learning Rationales (CLRs)

Objective 1: To familiarize the domains of supervised and unsupervised learning.

Objective 2: To understand and apply various binary classifiers.

Objective 3: To understand and apply clustering methods.

Objective 4: To understand and analyze Feedforward neural networks and CNNs

Objective 5: Able to work on real time projects related to AI/ML

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course, the learner will be able to	**Bloom's Level**	**Expected Proficiency Percentage**	**Expected Attainment Percentage**
Outcome 1	Familiarize supervised and unsupervised learning	1	85%	80%
Outcome 2	Understand and Apply various binary classifiers	1, 2	80%	75%
Outcome 3	Understand and Apply clustering methods	1, 2	85%	70%
Outcome 4	Understand and Evaluate Feedforward neural networks	3	80%	70%
Outcome 5	Understand the CNNs and able to work on real time projects	2,3,4	75%	70%

Course Articulation Matrix: (CLO) to Program Learning Outcomes (PLO)

CLO	**Program Learning Outcomes (PLO)**

	Engineering Knowledge	Problem Analysis	Design and Development	Analysis, Design and Research	Modern Tool and ICT Usage	Society and Multicultural Skills	Environment and Sustainability	Moral, and Ethical Awareness	Individual and Teamwork Skills	Communication Skills	Project Management and Finance	Self-Directed and Lifelong Learning	PSO1	PSO2	PSO3
Outcome 1	1	1	1	1	1							1	1	1	1
Outcome 2	2	3	2	3	2				2	1		1	1	2	3
Outcome 3	2	2	2	3	3				2	1		1	1	2	2
Outcome 4	2	3	3	3	3				2	1		1	2	3	3
Outcome 5	3	3	2	3	3				2	1		2	2	2	2
Course Average	**2**	**3**	**2**	**3**	**3**				**2**	**1**		**1**	**1**	**2**	**2**

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit 1	**Introduction**	**6**		
	Introduction to machine learning	1	1	1, 2,3
	Supervised learning	1	1	1, 2,3
	Unsupervised learning	1	1	1, 2,3
	Linear regression	2	1	1, 2,3
	Logistic regression	1	1	1, 2,3

Unit 2	**Classifiers**	**7**		
	Naive Bayes	1	2	1, 2,3
	Support Vector Machines	2	2	1, 2,3
	K-Nearest Neighbor	1	2	1, 2,3
	Decision Trees	2	2	1, 2,3
	Random forest	1	2	1, 2,3
Unit 3	**Clustering**	**6**		
	Clustering in machine learning	1	3	1, 2,3
	Different types of clustering algorithms	1	3	1, 2,3
	K-Means clustering	2	3	1, 2,3
	Loss functions in regression and classification	1	3	1, 2,3
	Bias-variance trade off	1	3	1, 2,3
Unit 4	**Feedforward neural networks**	**7**		
	Introduction to Neural Networks	1	4	1, 2,3
	Activation functions	1	4	1,2,3
	Feed-forward Network	2	4	1, 2,3
	Backpropagation algorithm	2	4	1, 2,3
	Introduction to convolutional neural network (CNN)	1	5	1, 2,3
Unit 5	**Applications of AI/ML**	**6**		
	Applications in VLSI	3	5	4
	Applications in IoT	3	5	4
Total Contact Hours		**45**		

Recommended Resources

1. Christopher M. Bishop, "Pattern Recognition and Machine Learning" by Springer, 2007.
2. Tom M. Mitchell, "Machine Learning", First Edition by Tata McGraw-Hill Education, 2013.
3. Luis G. Serrano, "Grooking Machine Learning" 2nd Edition, Manning Publications, 2021.
4. Reference papers from various journals such as IEEE, Elsevier etc.

Learning Assessment

	Continuous Learning Assessments (50%)	

Bloom's Level of Cognitive Task		CLA-1 (10%)		Mid-1 (15%)		CLA-2 (10%)		CLA-3 (15%)		End Semester Exam (50%)	
		Th	Prac	Th	Prac	Th	Prac	Th	Prac	Th	Prac
Level 1	Remember	40%	40%	60%	40%	40%	40%	60%	40%	30%	40%
	Understand										
Level 2	Apply	60%	60%	40%	60%	60%	60%	40%	60%	70%	60%
	Analyse										
Level 3	Evaluate										
	Create										
Total		**100%**		**100%**		**100%**		**100%**		**100%**	

Course Designer(s)

Dr. Sudhakar Tummala. Asst. Professor. And Dr. V. Udaya Sankar, Asst. Professor, Dept. Of ECE. SRM University – AP

Course Code	VLS 501	Course Category	Core Course	L-T-P-C	3	0	1	4
Pre-Requisite Course(s)		Co-Requisite Course(s)	CC	Progressive Course(s)				
Course Offering Department	ECE	Professional / Licensing Standards	*IEEE, Microsoft, Oracle, Max Planck Research etc.*					
Board of Studies Approval Date		Academic Council Approval Date						

Course Objectives / Course Learning Rationales (CLRs)

Objective 1: To understand the fundamental principles of CMOS technology, including the operation of MOS transistors, logic gates, and basic building blocks.

Objective 2: To learn the techniques for designing and analyzing CMOS digital circuits, including combinational and sequential logic circuits.

Objective 3: To gain proficiency in creating layout designs for CMOS circuits (considering area, power, and performance) and understand the importance of timing in digital circuits, and learn how to perform timing analysis for CMOS circuits.

Objective 4: To apply the knowledge gained in the course through hands-on projects that involve the design, simulation, and layout of CMOS digital circuits.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course, the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Understand the fundamental principles of CMOS Technology along with its advantages and limitations	2	85%	80%
Outcome 2	Design both combinational & sequential circuits using CMOS technology	3	80%	75%
Outcome 3	Create layout designs for CMOS digital circuits and understand the impact of the fabrication process on circuit design	3	85%	70%
Outcome 4	Apply theoretical knowledge to real-world digital IC design projects	3	80%	70%

Course Articulation Matrix: (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tool Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Team Work	Communication	Life-long Learning	PSO1	PSO2	PSO3
Outcome 1	**3**	**2**	**2**	**2**	**2**	**3**	**2**	**2**	**2**	**3**	**3**	**2**	**2**
Outcome 2	**3**	**3**	**3**	**2**	**2**	**1**	**2**	**2**	**3**	**3**	**2**	**3**	**2**
Outcome 3	**3**	**3**	**3**	**3**	**2**	**1**	**2**	**2**	**3**	**2**	**3**	**3**	**2**
Outcome 4	**3**	**3**	**3**	**3**	**2**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
Course Average	**3**	**3**	**3**	**2**	**2**	**2**	**2**	**2**	**3**	**3**	**3**	**3**	**2**

Course Unitization Plan -Theory

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References
Unit 1	**MOSFET Introduction and Layout of CMOS Logic Circuits**	**9**		
1.	Basic MOSFET Characteristics– Threshold Voltage, Body Bias concept, Current- Voltage Characteristics – Square-Law Model	2	1	1,2
2.	MOSFET Modeling– Drain-Source Resistance, MOSFET Capacitances	1	1	1,2
3.	Geometric Scaling Theory– Full-Voltage Scaling, Constant-Voltage Scaling, Challenges of MOSFET Scaling	2	1	1,2
4.	CMOS fabrication processing steps	1	1	1,2,4,6
5.	Design Rules, Stick diagram, Layout of logic circuits	2	1,3	
6.	Layout of logic circuits, latch-up	1	1,3	1,2,4,6
Unit 2	**Switching Properties of MOSFET and CMOS Inverter**	**8**		

7.	Static and dynamic characteristics of Pass Transistors	1	1,2	1,2
8.	Transmission Gate, TG based logic circuits, Introduction to CMOS Inverter	2	1,2	1,2
9.	CMOS Inverter - DC Characteristics, Noise Margins, Layout Considerations	1	1,2	1,2
10.	Inverter Switching Characteristics, Transient Effects on the VTC, RC Delay Modeling, Elmore Delay, Output Capacitance	2	1,2	1,2
11.	Inverter Design – DC Design, Transient Design, Driving Large Capacitive Loads	2	1,2	1,2
Unit 3	**Static CMOS Logic Elements & Power Dissipation in CMOS Logic Circuits**	**9**		
12.	CMOS NAND Gate, CMOS NOR Gate	1	2,3	1,2,3
13.	CMOS AND, OR, NOT, and Complex Logic Functions	2	2,3	1,2,3
14.	CMOS SRAM and DRAM Cell	1	2,3	1,2,3
15.	Dynamic Power Dissipation– Switching Power Dissipation	2	2,3	1,2,3
16.	Short Circuit Power Dissipation, Glitching Power Dissipation	1	1,3	1,2,3
17.	Static Power Dissipation, Diode Leakage Current, Subthreshold Leakage Current	2	1,3	1,2,3
Unit 4	**Dynamic Logic Circuit Concepts and CMOS Dynamic Logic Families**	**9**		
18.	Charge Leakage in CMOS circuits	2	2,4	1,2,5
19.	Charge Sharing, Dynamic RAM Cell	2	2,4	1,2,5
20.	Clocked-CMOS	2	2,4	1,2,5
21.	Pre-Charge/ Evaluate Logic, Domino Logic	2	2,4	1,2,5
	CMOS Single-Phase Logic	1	2,4	1,2,5
Unit 5	**Issues In Chip Design**	**8**		
22.	ESD Protection	2	2,3,4	1,2,5
23.	On-Chip Interconnects – Line Parasitics	1	2,3,4	1,2,5
24.	Modeling of the Interconnect Line	2	2,3,4	1,2,5
25.	Clock Distribution	2	2,3,4	1,2,5
26.	Input-Output circuits	1	2,3,4	1,2,5
	Total	**43**		

Recommended Resources

1. Rabaey, J.M., Chandrakasen, A.P. and Nikolic, B., Digital Integrated Circuits – A Design perspective, Pearson Education (2007) 2nd ed.
2. Kang, S. and Leblebici, Y., CMOS Digital Integrated Circuits – Analysis and Design, Tata McGraw Hill
3. J P Uyemura, CMOS Circuit Design, Springer
4. Weste, N.H.E. and Eshraghian, K., CMOS VLSI Design: A Circuits and Systems Perspective, eddision Wesley (1998) 2nd ed.
5. Baker, R.J., Lee, H. W. and Boyce, D. E., CMOS Circuit Design, Layout and Simulation, Wiley - IEEE Press (2004) 2nd ed.

6. Weste, N.H.E., Harris, D. and Banerjee, A., CMOS VLSI Design, Dorling Kindersley (2006) 3rd ed.

Other Resources

1. James D. Plummer, Michael D. Deal, Peter B. Griffin, Silicon VLSI Technology: Fundamentals, Practice and Modeling, Pearson Education, 2009.

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)				End Semester Exam (50%)
		CLA-1 (10%)	Mid-1 (15%)	CLA-2 (15%)	CLA-3 (10%)	
Level 1	Remember	40%	60%		50%	30%
	Understand					
Level 2	Apply	60%	40%	20%	50%	60%
	Analyse					
Level 3	Evaluate			80%		10%
	Create					
Total		**100%**	**100%**	**100%**	**100%**	**100%**

Course Designer(s)

Dr. M. Durga Prakash, *Asst. Professor. Dept. Of ECE. SRM University - AP*

Course Code	VLS 502	Course Category	Core Course (CC)	L-T-P-C	3	0	1	4
Pre-Requisite Course(s)		Co-Requisite Course(s)	VLSI Analog IC Design	Progressive Course(s)				
Course Offering Department	ECE	Professional / Licensing Standards	*IEEE, Microsoft, Oracle, Max Planck Research etc.*					

Course Objectives / Course Learning Rationales (CLRs)

Objective 1: To understand the fundamentals of Analog IC Design, including the single-stage amplifiers and Differential Amplifiers

Objective 2: To learn the general considerations for Operational Amplifiers designing and performance of various Op-Amp topologies

Objective 3: To understand the stability in feedback systems and noise in mixed signal IC design

Objective 4: To apply the data converters knowledge gained in the course through hands-on projects that involve the design, simulation, and layout of CMOS analog circuits.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course, the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Understand the fundamental of analog IC Design, including the single-stage amplifiers and Differential Amplifiers	2	85%	80%
Outcome 2	Design operational amplifiers and performance of various Op-Amp topologies	3	80%	75%
Outcome 3	Create layout designs for operational amplifier circuits and understand the stability in feedback system and noise performance	3	85%	70%
Outcome 4	Apply theoretical knowledge to real-world analog and digital converter IC design projects	3	80%	70%

Course Articulation Matrix: (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions	Conduct Investigations of Complex Problems	Modern Tool Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Team Work	Communication	Life-long Learning	PSO1	PSO2	PSO3
Outcome 1	**3**	**2**	**2**	**2**	**2**	**3**	**2**	**2**	**2**	**3**	**3**	**2**	**2**
Outcome 2	**3**	**3**	**3**	**2**	**2**	**1**	**2**	**2**	**3**	**3**	**2**	**3**	**2**
Outcome 3	**3**	**3**	**3**	**3**	**2**	**1**	**2**	**2**	**3**	**2**	**3**	**3**	**2**
Outcome 4	**3**	**3**	**3**	**3**	**2**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
Course Average	**3**	**3**	**3**	**2**	**2**	**2**	**2**	**2**	**3**	**3**	**3**	**3**	**2**

Course Unitization Plan -Theory

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References
Unit 1	**Introduction to Analog Integrated Design**	**10**		
1.	Models for analog design, body transconductance, Single-stage Amplifiers – CS stage, diode connected load	2	1	1,2
2.	Current source load and source degeneration Review of CD and CG stages	2	1	1,2
3.	Cascode stage & folded Cascode concepts	1	1	1,2
4.	Design of amplifier from specifications Differential Amplifiers	1	1	1,2,4
5.	MOS differential pair, Small signal operation. half circuit analysis common mode response	2	1,3	
6.	Differential amplifier with active load, common mode gain, and CMRR. Frequency response of the differential amplifier.	2	1,3	1,2,4
Unit 2	**Operational Amplifiers**	**10**		
7.	General considerations – performance parameters	1	1,2	1,2

8.	One-Stage Op amps – Cascode Op-Amps Telescopic Op-Amps	2	1,2	1,2
9.	Folded Cascode Op-Amps	1	1,2	1,2
10.	Two-Stage Op amps, Gain boosting	1	1,2	1,2
11.	Comparison of performance of various Op-Amp topologies	2	1,2	1,2
12.	Design of Op-Amps from specifications.	2	1,2	1,2
13.	Review of bode rules	1	1,2	1,2
Unit 3	**Stability In Feedback Systems**	**9**	1,2	1,2
15.	Problem of instability, Stability condition	1	2,3	1,2,3
16.	Gain-phase crossovers, phase margin	2	2,3	1,2,3
17.	Frequency compensation: frequency response of cs amplifier, Miller effect	1	2,3	1,2,3
18.	Poles in a system, Pole-splitting, miller compensation	2	2,3	1,2,3
19.	Two-stage Op-Amp - compensation techniques	1	1,3	1,2,3
20.	Closed-loop stability, optimal phase margin.	2	1,3	1,2,3
Unit 4	**Noise**	9		
21.	MOSFET noise models, types of noise, thermal noise, flicker noise	2	2,4	1,2,5
22.	Representation of noise in circuits, Noise in single-stage amplifiers	2	2,4	1,2,5
23.	Integrated Oscillators: Ring oscillators	2	2,4	1,2,5
24.	LC oscillators – Cross coupled oscillators, VCO.	2	2,4	1,2,5
Unit 5	**Data Converters**	**7**		
25.	DAC and ADC Specifications, Current Steering DAC	2	2,3,4	1,2,5
26.	Charge Scaling DAC, Cyclic DAC	2	2,3,4	1,2,5
27.	Pipeline DAC, Flash ADC	2	2,3,4	1,2,5
28.	Pipeline ADC, Integrating ADC, Successive Approximation ADC.	2	2,3,4	1,2,5
	Total	**45**		

Recommended Resources

1. Design of Analog CMOS Integrated Circuits, Behzad Razavi, 2002, Mc GrawHill Edition, ISBN: 0-07- 238032-2.
2. CMOS Circuit Design, Layout and Simulation, R. Jacob Baker, Harry W. Li and David E. Boyce, 2002, IEEE Press, ISBN: 81-203-1682-7.
3. CMOS Mixed-signal Circuit Design, R. Jacob Baker, 2009, IEEE Press, ISBN: 978- 81-265-1657-5.
4. Analysis and Design of Analog Integrated Circuits, Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, "", 4th edition, 2008, Wiley India Private Limited, ISBN:978-8126515691.
5. Fundamentals of Microelectronics, Behzad Razavi, 2nd Edition, 2013, Wiley, ISBN- 10: 1118156323

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)				End Semester Exam (50%)
		CLA-1 (10%)	Mid-1 (15%)	CLA-2 (15%)	CLA-3 (10%)	
Level 1	Remember	40%	60%		50%	30%
	Understand					
Level 2	Apply	60%	40%	20%	50%	60%
	Analyse					
Level 3	Evaluate			80%		10%
	Create					
Total		**100%**	**100%**	**100%**	**100%**	**100%**

Course Designer(s)

a. ***Dr. M. Durga Prakash****. Asst. Professor. Dept. Of ECE. SRM University - AP*

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Neerukonda, Mangalagiri Mandal
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VLSI Technology

Course Code	**VLS 503**	**Course Category**	**CC**	**L-T-P-C**	3 1 0 4
Pre-Requisite Course(s)		**Co-Requisite Course(s)**		**Progressive Course(s)**	
Course Offering Department	**ECE**	**Professional / Licensing Standards**	*IEEE, Microsoft, Cadence*		
Board of Studies Approval Date		**Academic Council Approval Date**			

Course Objectives / Course Learning Rationales (CLRs)

Objective 1: To study the various processes of IC fabrication.

Objective 2: To study the device fabrication process.

Objective 3: To understand various issues of defects and stresses in the films.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course, the learner will be able to	**Bloom's Level**	**Expected Proficiency Percentage**	**Expected Attainment Percentage**
Outcome 1	Outline the basics of semiconductor crystal properties	2	80%	75%
Outcome 2	Identify the fundamentals of IC fabrication	3	80%	75%
Outcome 3	Illustrate the different methods involved in VLSI fabrication process.	4	80%	75%
Outcome 4	Appreciate the advanced methods involved in IC fabrication.	4	80%	75%
Outcome 5	Build the knowledge of process integration-of devices	4	80%	75%
Outcome 6	Build the knowledge of Packaged the devices	4	80%	75%

Course Articulation Matrix: (CLO) to Program Learning Outcomes (PLO)

CLOs

	Engineering Knowledge	Design and Development of Solutions	Conduct Investigations of Complex Problems	Modern Tool Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork	Communication	Lifelong Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	1	1	2	2	2	2	2	2	2	2	2	2
Outcome 2	3	1	1	2	2	2	2	2	2	2	2	2	2
Outcome 3	2	3	3	2	3	3	3	2	3	2	3	3	3
Outcome 4	2	3	3	2	3	3	3	3	3	1	3	3	3
Outcome 5	2	3	3	2	3	3	3	3	3	2	3	3	3
Outcome 6	2	3	3	2	3	3	3	3	3	1	3	3	3
Course Average	**2**	**3**	**3**	**2**	**3**	**3**	**3**	2	**3**	**2**	**3**	**3**	**3**

Course Unitization Plan -Theory

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References
Unit 1	**Clean Room Environment and Wafer Preparation**	**10**		
1.	Crystal Structure of a solid	1	1	1,2
2.	Defects in materials	1	1	1,2
3.	Types of clean room, Contamination in clean room	2	1,2	1,2
4.	Electronic Grade Silicon, Czochralski crystal growing	2	1,2	1,2,4,6
5.	Silicon Shaping	2	1,2	
6.	Wafer cleaning processes and wet chemical etching techniques	2	1,2	1,2,4,6
Unit 2	**Oxidation, Diffusion, and Implantation**	**12**		
7.	Kinetics of Silicon dioxide growth both for thick, thin, and ultrathin films	3	2,3	1,2
8.	Oxidation Techniques and Systems Models of Diffusion in Solids	2	2,3	1,2

9.	Defects due to oxidation	2	1,2,3	1,2
10.	Solid State diffusion modelling and technology	2	1,2,3	1,2
11.	Implantation Equipment, Principles, techniques and applications	2	2,3	1,2
12.	Removal of implant damage	1	2,3	
Unit 3	**Epitaxial Growth, Metallization**	**12**		
13.	CVD and MBE	3	2,3	1,2,3
14.	Defects in Epitaxial Layer Dielectric Deposition	2	2,3	1,2,3
15.	PECVD and Rapid Thermal Annealing	2	2,3,4	1,2,3
17.	E-beam evaporation	2	2,3,4	1,2,3
18.	Sputtering and Thermal Evaporation	2	2,3	1,2,3
19.	Etching	1	2,3,4	1,2,3
Unit 4	**Lithography**	**6**		
20.	Optical Lithography	2	2,3,4	1,2,5
21.	E-beam lithography	2	2,3,4	1,2,5
22.	X-ray	1	2,3,4	1,2,5
23.	Other Lithography techniques	1	2,3,4	1,2,5
Unit 5	**Fabrication and Packaging**	**5**		
24.	Fabrication of MOSFET	2	3,4,5	1,2,5
25.	Process to Package a chip (Dicing, Attaching, wire bonding, Chip package header)	2	2,3,4	1,2,5
26.	Fabrications of other devices	1	2,3,4	1,2,5
	Total	**45**		

Learning Assessment (Theory)

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)				End Semester Exam (50%)
		CLA-1 (15%)	Mid-1 (15%)	CLA-2 (10%)	CLA-3 (10%)	
Level 1,2	Understand	40%	40%	20%	30%	30%
	Apply					
Level 2,3	Understand	40%	40%	40%	30%	50%
	Apply					
Level 3,4	Apply	20%	20%	40%	40%	20%
	Analyse					
Total		**100%**	**100%**	**100%**	**100%**	**100%**

Course Designer(s)

Dr. Manas Ranjan Tripathy*. Asst. Professor. Dept. Of ECE. SRM University – AP*

VLSI Physical Design

Course Code	VLS 504	Course Category	Technical Elective(TE)	L-T-P-C	3	0	1	4
Pre-Requisite Course(s)	VLSI Design	Co-Requisite Course(s)		Progressive Course(s)				
Course Offering Department	ECE	Professional / Licensing Standards						
Board of Studies Approval Date		Academic Council Approval Date						

Course Objectives / Course Learning Rationales (CLRs)

Objective 1: To understand the requirements of VLSI automation Tools.
Objective 2: To understand the requirements Proper placement and Routing of Circuits.
Objective 3: To familiarize with methods and algorithms for efficient Floor Planning and Routing
Objective 4: To understand different circuit level techniques for logic synthesis.
Objective 5: To understand how high-level synthesis is carried out for proper allocation, scheduling and assignment.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Describe various VLSI Automation Tools	2	70%	65%
Outcome 2	Implement ideas on Placement and Partitioning of Circuits	3	70%	65%
Outcome 3	Identify concepts and Algorithms of Floor planning and Routing	3	70%	65%
Outcome 4	Develop circuit level techniques and apply in logic Synthesis	3	70%	65%
Outcome 5	Working on High Level Synthesis of Circuits	4	70%	65%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)														
	Engineering Knowledge	Problem Analysis	Design and Development	Analysis, Design and Research	Modern Tool and ICT Usage	Society and Multicultural Skills	Environment and Sustainability	Moral, and Ethical Awareness	Individual and Team work Skills	Communication Skills	Project Management and Finance	Self-Directed and Life Long Learning	PSO1	PSO2	PSO3
Outcome 1	3	3	3	2	1		2					3	3	1	2
Outcome 2	3	3	3	2	2	1	2		3			2	3	2	2
Outcome 3	3	3	3	2	2		2		3			3	3	2	2

Outcome 4	3	3	3	3	2	1	2		3			2	3	2	2
Outcome 5	3	3	3	2	2	1	2		2			2	3	2	2
Course Average	**3**	**3**	**3**	**2**	**2**	**1**	**2**		**3**			**2**	**3**	**2**	**2**

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit 1	**VLSI DESIGN AUTOMATION TOOLS**	**16**		
1.	Algorithms and system design, Structural and logic design	2	1	1
2.	Transistor level design, Layout design	2	1	1
3.	Verification methods	1	1	1
4.	Design management tools	1	1	1
5.	Layout compaction	2	2	1
6.	placement and routing, Pin Assignment	2	2	1
7.	Design rules, symbolic layout, Applications of compaction	2	2	2
8.	Formulation methods, Algorithms for constrained graph compaction	2	2	2
9.	Circuit representation, Wire length estimation, Placement algorithms, Partitioning algorithms	2	2	2
Unit 3	**FLOOR PLANNING AND ROUTING**	**10**		
10.	Floor planning concepts	2	3	1,2
11.	Shape functions and floor planning sizing	2	3	1,2
12.	Local routing, Area routing	2	3	1,2
13.	Channel routing	2	3	1,2
14.	Global routing and its algorithms.	2	3	1,2
Unit 4	**SIMULATION AND LOGIC SYNTHESIS**	**10**		
15.	Gate level and switch level modelling and simulation	1	4	2,3

16.	Introduction to combinational logic synthesis	1	4	2,3
17.	STA	2	4	2,3
18.	ROBDD principles, Implementation, construction and manipulation	2	4	2,3
19.	Two level logic synthesis.	2	4	3,4
20.	Timing Closure	2	4	3,4
Unit 5	**HIGH-LEVEL SYNTHESIS**	**11**		
21.	Hardware model for high level synthesis	2	5	3,4
22.	Internal representation of input algorithms	1	5	3,4
23.	Allocation, assignment, and scheduling	2	5	3,4
24.	Scheduling algorithms, Aspects of assignment	1	5	3,4
25.	High level transformations	1	5	3,4
	Total	**47**		

Recommended Resources

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley ,1998.
2. N.A.Sherwani , "Algorithms for VLSI Physical Design Automation", (3/e), Kluwer,1999..
3. S.M. Sait , H. Youssef, "VLSI Physical Design Automation", World scientific, 1999
4. cadence.com/content/dam/cadence-www/global/en_US/documents/tools/digital-design-signoff/innovus-implementation-system-ds.pdf

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (60%)								End Semester Exam (40%)	
		CLA-1 (15%)		Mid-1 (15%)		CLA-2 (15%)		Mid-2 (15%)			
		Th		Th		**Th**		**Th**		**Th**	
Level 1	Remember	60%		50%		60%		50%		40%	
	Understand										
Level 2	Apply	40%		50%		40%		50%		60%	
	Analyze										
Level 3	Evaluate										
	Create										
Total		**100%**		**100%**		**100%**		**100%**		**100%**	

Course Designers

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SEMESTER II

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Entrepreneurial Mindset

Course Code	**SEC 103**	Course Category	**SEC**	L-T-P-C	1	0	1	2
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)				
Course Offering Department	**Management**	Professional / Licensing Standards	-					
Board of Studies Approval Date		Academic Council Approval Date						

Course Objectives / Course Learning Rationales (CLRs)

Objective 1: To develop the Entrepreneurial Mindset of Students
Objective 2: To provide students an overview of different aspects of starting a business

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	**Bloom's Level**	**Expected Proficiency Percentage**	**Expected Attainment Percentage**
Outcome 1	**Recall** the key entrepreneurship concepts and entrepreneurial traits	1	90%	80%
Outcome 2	Identify entrepreneurial opportunities	2	80%	80%
Outcome 3	**Apply** entrepreneurial skills to analyze different entrepreneurial ventures.	3	70%	70%
Outcome 4	Apply entrepreneurial concepts to and develop a business model canvas	3	60%	60%

Course Articulation Matrix (CLO) to (PLO)

3 = High, 2 = Medium, 1 = Low

CLOs	**Program Learning Outcomes (PLO)**													
	Management Knowledge	Analytical Reasoning and Problem Solving	Critical and Reflective Thinking	Strategic Thinking and Logical Reasoning	Modern Tools and ICT Usage	Environment and Sustainability	Moral, Multicultural and Ethical Awareness	Individual and Teamwork Skills	Communication Skills	Leadership Readiness Skills	Self-Directed and Lifelong Learning	PSO1	PSO2	PSO3

Outcome 1	3			2				2		2	2			
Outcome 2	1	3	3	3				3			3			
Outcome 3	2	3	3	3				3		2	3			
Outcome 4	3	3	3	3				3		3	3			
Course Average	**2**	**3**	**3**	**3**				**3**		**2**	**3**			

Course Unitization Plan - Theory

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit 1	**Introduction**	**2**	**1,3**	
1.	What is Entrepreneurship			
2.	Challenges Faced by Entrepreneurs			
3.	Why not entrepreneurship			
4.	Who is an Entrepreneurs (Characteristics and Myths)			
5.	Why become entrepreneurs			
6.	Entrepreneurial Traits			
7.	Significance of entrepreneurship in the economy			
8.	Types of Entrepreneurial Ventures			
Unit 2	**Entrepreneurial Orientation**	4	1,2,4	
9.	Characteristics of successful entrepreneurs			
10.	Mindset shifts: from an employee to an entrepreneur			
11.	Overcoming challenges and dealing with failures			
Unit 3	**Entrepreneurial Skills**	**4**	1,2,3,4	
12.	Innovation & Creativity			
13.	Design Thinking			
14.	Strategic Thinking			
15.	Developing a Growth Mindset			
Unit 4	**Technopreneurship**	**2**	1,2	
16.	Overview of Technopreneurship			
17.	Characteristics of a Technopreneur			
18.	Technology Trends and Disruption			
19.	Real-world Technopreneurship Examples			

Unit 5	**Entrepreneurial Opportunity & Ideation**	4	2	
20.	Difference between idea and opportunity			
21.	Opportunities in Vibrant Indian Entrepreneurial Ecosystem			
22.	Opportunity Recognition (Sources of Opportunity)			
23.	Assessing Opportunity			
24.	Opportunities and Uncertainty			
25.	Idea Generation & Market Research			
26.	Idea Selection			
Unit 6	Business Model Canvas & Pitching	2	1,4	
27.	Why BMC			
28.	Value Proposition			
29.	Customer Discovery			
30.	Customer Relationship			
31.	Channels			
32.	Key Partners			
33.	Key Activities			
34.	Key Resources			
35.	Revenue Structure			
36.	Cost Structure			
37.	From Pitch to Hitch (Pitch Deck)			
Unit 7	Startup Financing	2	1,4	
38.	Stages of Fund Raising			
39.	Startup Valuation			
40.	Mode of Investment			
41.	Shareholder's Agreement			
42.	Financial Analysis			
Total Contact Hours		**20**		

Recommended Resources

1. Larry Keeley Brian Quinn Ryan Pikkel. Ten types of innovation -the discipline of building breakthroughs, John Wiley& Sons, Inc; 2013
2. Eric Ries. The lean startup how constant innovation creates radically successful businesses, Penguin Books
3. Bruce R. Barringer, R. Duane Ireland. Entrepreneurship Successfully Launching New Ventures, Pearson; 2020
4. Robert D. Hasrich, Dean A. Shepherd, Michael P. Peters, Entrepreneurship, McGraw Hill, 2020
5. Siva Prasad N. Design Thinking : Techniques And Approaches, Ane Books, New Delhi; 2023

Other Resources

Coursera:
https://www.coursera.org/specializations/innovation-creativity-entrepreneurship
https://www.coursera.org/specializations/wharton-entrepreneurship

Learning Assessment (Theory)

Bloom's Level of Cognitive Task		Continuous Learning Assessments (100%)		
		CLA-1 (30%)	CLA-2 (30%)	CLA-3 (40%)
Level 1	Remember	100%	40%	
	Understand			
Level 2	Apply		60%	100%
	Analyse			
Level 3	Evaluate			
	Create			
Total		**100%**	**100%**	**100%**

Course Designers

a. **Mr Aftab Alam,** Assistant Professor, Paari School of Business, SRM University-AP
b. **Mr Udayan Bakshi,** Associate Director, Entrepreneurship and Innovation, SRM University-AP
c. **Prof. Bharadhwaj S,** Dean, Paari School of Business, SRM University-AP

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VLSI TESTING AND VERIFICATION

Course Code	VLS 505	Course Category	Core Course (CC)	L-T-P-C	3	0	1	4
Pre-Requisite Course(s)	ENG 211 ECE 320	Co-Requisite Course(s)		Progressive Course(s)				
Course Offering Department	ECE	Professional / Licensing Standards						
Board of Studies Approval Date		Academic Council Approval Date						

PURPOSE: To provide necessary knowledge and skills to ensure the successful design, manufacturing, and deployment of highly reliable and efficient integrated circuits in modern electronic devices

COURSE OBJECTIVES / COURSE LEARNING RATIONALES (CLRS):

Objective 1 (To ensure Quality and Reliability): As VLSI circuits become more complex and denser, the likelihood of defects and errors increases. Testing and verification techniques are employed to ensure that the fabricated chips meet the desired specifications and are free from manufacturing defects. This is crucial to ensure the overall quality and reliability of the integrated circuits used in various electronic devices.

Objective 2 (To detect and Fix Design Errors): During the design phase of VLSI circuits, errors and bugs can be introduced inadvertently. Proper testing and verification processes help identify these design errors early in the development cycle. This allows designers to correct the mistakes before the chips are manufactured; thus, saving time and costs associated with rework.

Objective 3 (Functional Verification): VLSI circuits are designed to perform specific functions. This subject is focused on verifying that these functions are correctly implemented and that the chip behaves as intended under various operating conditions.

Objective 4 (Performance Analysis): VLSI Testing and Verification also involve assessing the performance of the integrated circuits. This includes verifying that the chips meet the required speed, power, and area constraints specified during the design phase.

Objective 5 (To know about the Test Methodologies and Techniques): This subject will also cover various test methodologies and techniques used to evaluate the performance and functionality of VLSI circuits. This includes design for testability (DFT), built-in self-test (BIST), automatic test pattern generation (ATPG), and scan-based testing, among others.

Objective 6 (Fault Models and Test Coverage): Understanding and dealing with different fault models are essential for designing effective tests to identify potential defects in VLSI circuits. This subject will cover various fault models and techniques to achieve high test coverage.

Objective 7 (Manufacturability and Yield Enhancement): Testing and verification are critical for assessing the manufacturability of VLSI circuits and improving yield during the chip fabrication process. A higher yield means fewer defective chips, leading to cost savings and better overall productivity.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course, the learner will	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Have a solid understanding of testing methodologies, verification techniques, and design-for-testability principles	2	80%	70%
Outcome 2	Acquire confidence to work on real-world projects, use industry-standard tools, and simulate various testing scenarios	3	80%	70%
Outcome 3	Gain insights into the current trends and challenges in VLSI Testing and Verification, such as dealing with increased complexity, power constraints, and manufacturing defects	4	75%	65%
Outcome 4	Be able to explore career opportunities in the semiconductor industry, particularly in roles related to design verification, validation, and test engineering	4	70%	60%

Course Articulation Matrix: (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions Conduct Investigations of Complex Problems	Conduct Investigations of Complex Problems	Modern Tool Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Team Work	Communication	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	2	2	2	3	2	2	1	3	3	3	2	3	2
Outcome 2	3	3	2	3	2	2	1	2	2	3	2	3	2
Outcome 3	3	3	2	3	2	2	1	3	2	3	2	3	2
Outcome 4	3	2	2	2	2	2	1	3	2	3	2	3	3
Course Average	**3**	**3**	**2**	**2**	**2**	**2**	**1**	**3**	**2**	**3**	**2**	**3**	**2**

Course Unitization Plan

Unit No.	Description of Topic	Required Contact Hours	CLOs addressed	References Used
Unit 1	**INTRODUCTION TO VLSI TESTING**	**7**	1, 3	1, 2
1.	VLSI design flow	1		
2.	Overview of Verification and Testing			
3.	Need of pre-silicon verification			
4.	Need of post-silicon validation and debug			
5.	VLSI Testing needs and challenges	1		
6.	Possible Outcome of Testing			
7.	Stages of IC Product			
8.	Types of Testing: Implicit, Explicit			

9.	Production Test	1		
10.	Characterization Test	1		
11.	Reliability Test	1		
12.	Test Quality Measures	1		
13.	Yield and defects			
14.	Scope of testing and verification in VLSI design process	1		
15.	Issues in test and verification of complex chips			
Unit 2	**FAULT MODELING AND FAULT SIMULATION**	**12**	1, 3	3, 4, 7, 8
16.	Overview of Defect, Fault, Error, Failure	1		
17.	Random and Systematic defects			
18.	Overview of Test pattern, Test Set, Test Length, Fault Coverage			
19.	Importance of Fault modeling			
20.	Introduction to Fault models	1		
21.	Single stuck-at-fault model			
22.	Fanout stem and branch for Stuck-at-fault model			
23.	Multiple stuck at fault	1		
24.	Bridging faults			
25.	Bridging fault models: Wired-OR, Wired-AND, A-Dominant	2		
26.	Feedback bridging faults	2		
27.	Fanout Stem and Branch for Bridge Fault			
28.	Permanent and Transient Bridge Fault			
29.	Delay fault and its detection	2		
30.	Delay fault models Introduction			
31.	Path delay fault: Falling transition, Rising transition			
32.	Transition delay fault: Slow-to-rise (STR) and slow-to-fall (STF)	1		
33.	Overview of Transistor level or Switch level fault model	1		
34.	Stuck-open fault			
35.	Stuck-short fault			
36.	Fault Simulation Overview	1		
37.	Yield and Fault Equivalence			
Unit 3	**TESTABILITY MEASURES AND ANALYSIS**	**6**	1, 3, 4	2, 7
38.	Introduction and need of testability measures	1		
39.	Testability Components: Controllability and Observability			
40.	Overview of Testability Analysis			
41.	Topology-based Analysis	2		
42.	SCOAP: Combinational Controllability and Combinational Observability			
43.	Probability-based Analysis	2		
44.	COP: Combinational Controllability and Combinational Observability			
45.	High-level Analysis	1		
Unit 4	**ATPG AND DESIGN FOR TESTABILITY METHODS**	**14**	1, 2, 3	5, 6, 7, 8, 9

46.	Test pattern generation Overview: Random and Deterministic	1		
47.	Automatic test pattern generation: Complete and Incomplete ATPG			
48.	Combinational ATPG Introduction	2		
49.	Boolean Difference Method			
50.	SAT	1		
51.	Path-sensitization Method	2		
52.	Single Path Sensitization			
53.	Multiple Path Sensitization			
54.	D Algorithm	1		
55.	PODEM	1		
56.	FAN	1		
57.	Sequential ATPG Introduction	3		
58.	Scan design			
59.	Issues in Scan Design			
60.	Test interface and boundary scan			
61.	Iddq testing			
62.	Delay fault testing	2		
63.	Built-in Self-Test			
Unit 5	**VLSI DESIGN VERIFICATION**	**6**	3, 4	7, 8, 10
64.	Design verification techniques: Introduction	1		
65.	Techniques based on simulation approach			
66.	Techniques based on analytical approach	1		
67.	Techniques based on formal approach	1		
68.	Functional verification	3		
69.	Timing verification			
70.	Formal verification			
Total Contact Hours: 45				

TEXTBOOKS/REFERENCE BOOKS	
1	L.T. Wang, C.W. Wu, and X. Wen, "*VLSI Test Principles and Architectures*", Morgan Kaufmann, 2006
2	M.L. Bushnell and V.D. Agrawal, *"Essentials of electronic testing,"* Kluwer Academic Publishers, 2000
3	George W. Zobrist, VLSI Fault Modeling and Testing Techniques (VLSI Design Automation Series), Praeger Publishers Inc, 1993
4	RL Wadsack, "Fault modeling and logic simulation of CMOS and MOS integrated circuits" Bell System Technology, 1978
5	Hideo Fujiwara, Logic testing and design for testability, MIT Press, 1985
6	M. Abramovici, M. A. Breuer and A.D. Friedman, "*Digital systems testing and testable design*," IEEE Press,1994
7	P. K. Lala, "Digital Circuits Testing and Testability", Academic Press
8	Stephan Eggersgluss and Rolf Drechsler, High Quality Test Pattern Generation and Boolean Satisfiability, Springer, 2012
9	P.H. Bardell, W.H. McAnney, and J. Savior, "Built-in Test for VLSI: Pseudorandom Techniques," Wiely Interscience, 1987
10	Khosrow Golshan, Physical Design Essentials: An ASIC Design Implementation Perspective, Springer, 2007

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (60%)				End Semester Exam (40%)
		CLA-1 (15%)	Mid-1 (15%)	CLA-2 (10%)	CLA-3 (20%)	
Level 1	Remember	65%	50%	45%	60%	50%
	Understand					
Level 2	Apply	35%	50%	55%	40%	50%
	Analyse					
Level 3	Evaluate					
	Create					
Total		**100%**	**100%**	**100%**	**100%**	**100%**

Course Designer: Dr. Swagata Samanta, *Assistant Professor, Department of Electronics & Communication Engineering, SRM University – AP*

SRM University – AP, Andhra Pradesh

Neerukonda, Mangalagiri Mandal
Guntur District, Mangalagiri, Andhra Pradesh 522240

Semiconductor Device Modelling

Course Code	**VLS 506**	Course Category	**Speciality Stream Courses (CC)**	L-T-P-C	**3**	**0**	**1**	**4**
Pre-Requisite Course(s)	**Solid State Device Physics**	Co-Requisite Course(s)		Progressive Course(s)				
Course Offering Department	**ECE**	Professional / Licensing Standards						
Board of Studies Approval Date		Academic Council Approval Date						

Course Objectives / Course Learning Rationales (CLRs)

Objective 1: Learn the basics of current flow though solid state semiconductor devices.
Objective 2: Understand some elementary concepts of quantum- and statistical-mechanics.
Objective 3: Gain knowledge of electrostatics of P-N junction diodes.
Objective 4: Learn the design of Bipolar transistors.
Objective 5: Understand the design of MOSFETs
Objective 6: Apply theoretical knowledge of performance of BJTs and MOSFETs using ABACUS simulation tool.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	**Bloom's Level**	**Expected Proficiency Percentage**	**Expected Attainment Percentage**
Outcome 1	Identify current flow though semiconductor devices	2	70%	65%
Outcome 2	Identify concepts of quantum- and statistical-mechanics	2	70%	65%
Outcome 3	Discuss electrostatics of P-N junction diodes	3	70%	65%
Outcome 4	Discuss BJT and MOSFET design	3	70%	65%
Outcome 5	Illustrate the applications of MOSFETs design	3	70%	65%
Outcome 6	Demonstrate BJTs and MOSFETs design using ABACUS	3	70%	65%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	**Program Learning Outcomes (PLO)**											
	Engineering Knowledge	Design / Development of Solutions Conduct Investigations of Complex Problems	Conduct Investigations of Complex Problems	Modern Tool Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Team Work	Communication	Life-long Learning	PSO 1	PSO 2	PSO 3

Outcome 1	1	2	1	3	2	3	2	2	2	3	3	2	2
Outcome 2	1	2	2	3	2	1	2	2	3	3	2	3	2
Outcome 3	1	2	2	3	2	1	2	2	3	2	3	3	2
Outcome 4	1	2	2	3	2	3	3	3	3	3	3	3	3
Outcome 5	2	3	2	3									
Outcome 6	2	2	2	3									
Course Average	2	2	1	3	2	2	2	2	3	3	3	3	2

Course Unitization Plan- Theory

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit I	**Basic Semiconductor Properties & Elements of Quantum Mechanics**	**9**		
1.	General Material Properties	2	1	1,3
2.	Crystal Structure, The Unit Cell Concept	1	1	1,3
3.	Simple 3-D Unit Cells	1	2	1,3
4.	Bravais Lattices and Crystal Systems	1	3	1,3
5.	Specific Semiconductor Lattices	1	2	1,3
6.	Miller Indices, Example Use of Miller Indices	1	2	1,3
7.	The Quantum Concept	1	2	1,3
8.	Basic Formalism, Simple Problem Solutions	1	2	1,3
Unit II	**Energy Band Theory & Equilibrium Carrier Statistics**	**9**		
9.	Preliminary Considerations, Approximate One-Dimensional Analysis	2	1	1,4
10.	Extrapolation of Concepts to Three Dimensions	2	1	1,4
11.	Density of States, Fermi Function	1	2	1,4
12.	Equilibrium Distribution of Carriers	1	3	1,4
13.	The Energy Band Diagram, Donors	1	2	1,4
14.	Acceptors, Band Gap Centers	1	2	1,4

15.	Equilibrium Concentration Relationships, Concentration and E_F Calculations.	1	2	1,4
Unit III	**Recombination-Generation Processes & Carrier Transport**	**9**		
16.	Introduction	1	2	2,3
17.	Recombination-Generation Statistics	2	2	2,3
18.	Surface Recombination-Generation	2	2	2,3
19.	Supplemental R-G Information	1	2	2,3
20.	Drift	1	2	2,3
21.	Diffusion	1	2	2,3
22.	Equations of State	1	2	2,3
Unit IV	**Electrostatics of P-N Junction Diodes & Introduction to Bipolar Transistors**	**9**		
23.	P-N Diode I-V Characteristics	1	3	2,4
24.	Non-ideal Effects	1	3	2,4
25.	AC Response	1	3	2,4
26.	Large Signal Response	1	4	2,4
27.	Schottky Diode I	1	4	2,4
28.	Schottky Diode II	1	3	2,4
29.	BJT Design I	1	4,5,6	2,4
30.	BJT Design II	1	4,5,6	2,4
31.	Heterojunction Bipolar Transistors	1	4,5,6	2,4
Unit V	**MOS**	**9**		
32.	MOS Electrostatics	2	4	2,4
33.	MOSCAP Frequency Response	1	4	2,4
34.	MOSFET I-V Characteristics	2	4	2,4
35.	Nonideal Effects in MOSFET	2	4	2,4
36.	Modern MOSFET	1	3	2,4
37.	Reliability of MOSFET	1	3	2,4
Total Contact Hours		**45**		

Course Unitization Lab Plan - Tutorials

Session No.	Description of Experiments	Required Contact Hours	CLOs Addressed	References Used
1.	Interactive visualization of different Bravais lattices, and crystal planes, and materials (diamond, Si, InAs, GaAs, graphene, buckyball).	2	2	4,5
2.	Study of Band Models / Band Structure	2	3	4,5
3.	Carrier Distributions: demonstrates electron and hole density distributions based on the Fermi-Dirac and Maxwell Boltzmann equations	2	3,5,6	4
4.	Understand the basic concepts of DRIFT and DIFFUSION of carriers inside bulk semiconductors	2	3,5,6	4
5.	Simulate semiconductor process modeling	2	3,5,6	4
6.	Basic concept of PN Junction devices	2	3	4,5
7.	Study of Solar Cells	2	3	5

8.	Simulate npn and pnp Bipolar Junction Transistors (BJTs)	2	4	4,5
9.	Analysis of MOS Capacitors	2	4	4
10.	Implement MOSFET / Many-Acronym-Device-FET (mad-FETs)	4	4	4,5
Total Contact Hours		**22**		

Recommended Resources

1. Advanced Semiconductor Fundamentals, Second Edition, by Robert F. Pierret, Pearson Education, Inc. (1983).
2. Semiconductor Device Fundamentals, Robert F.Perret, (1996).
3. Sze, S. M., & Ng, K. K. (2006). Physics of semiconductor devices. John wiley& sons.
4. B. G. Streetman, S. K. Banerjee, Solid State Electronic Devices, Pearson, (2016)
5. Arora, N. (2007). MOSFET modeling for VLSI simulation: theory and practice. World Scientific.

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)					End Semester Exam (50%)	
		Theory (30%)				Practical (20%)		
		CLA-1 (5%)	Mid-1 (10%)	CLA-2 (5%)	Mid-2 (10%)		Th	Prac
Level 1	Remember	60%	40%	60%	40%	50%	30%	40%
	Understand							
Level 2	Apply	40%	60%	40%	60%	50%	70%	60%
	Analyse							
Level 3	Evaluate							
	Create							
Total		**100%**	**100%**	**100%**	**100%**	**100%**	**100%**	**100%**

Course Designers

a. ***Dr. M. Durga Prakash****, Assistant Professor, Department of ECE, SRM University – AP*

SRM University – AP, Andhra Pradesh

Neerukonda, Mangalagiri Mandal
Guntur District, Mangalagiri, Andhra Pradesh 522240

Advanced HDL based FPGA Design

Course Code	VLS 507	Course Category	CC	L-T-P-C	3	0	1	4

Pre-Requisite Course(s)		**Co-Requisite Course(s)**	**Digital system design**	**Progressive Course(s)**	
Course Offering Department	**ECE**	**Professional / Licensing Standards**			
Board of Studies Approval Date		**Academic Council Approval Date**			

Course Objectives / Course Learning Rationales (CLRs)

Objective 1: To study and understand the basic principles and concepts of electronic components, devices, and circuitry, specifically related to semiconducting P-N junction.

Objective 2: To understand and analyze the characteristics of P-N junction diodes and their applications in designing various electronic devices and circuits

Objective 3: To understand, analyze, and design the Bipolar-Junction (BJT) and Field-Effect transistors (FET) based electronic circuits followed by advanced Operational amplifier (Op-Amp) based circuits.

Objective 4: To apply the knowledge gained in the course to real-world applications and work on practical projects to reinforce theoretical concepts.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course, the learner will be able to	**Bloom's Level**	**Expected Proficiency Percentage**	**Expected Attainment Percentage**
Outcome 1	Define and understand the basic principles of electronic components related to semiconducting PN junction and other diodes.	2	85%	80%
Outcome 2	Understand, analyze and design the BJT & FET based electronic circuits	3	80%	75%
Outcome 3	Understand the properties of operational amplifiers, and their applications in designing and analyzing the various circuit operations (summing, integration, differentiation, filtering, etc).	3	80%	75%
Outcome 4	Apply the knowledge gained in the course to real-world applications and work on practical projects	4	75%	70%

Course Articulation Matrix: (CLO) to Program Learning Outcomes (PLO)

CLO	Program Learning Outcomes (PLO)														
	Engineering Knowledge	Problem Analysis	Design and Development	Analysis, Design and Research	Modern Tool and ICT Usage	Society and Multicultural Skills	Environment and Sustainability	Moral, and Ethical Awareness	Individual and Team work Skills	Communication Skills	Project Management and Finance	Self-Directed and Life long Learning	PSO1	PSO2	PSO3
Outcome 1	2	3	1	2	2				1	2	1	3	2	2	2
Outcome 2	2	3	2	3	2				2	2		3	2	3	3
Outcome 3	3	3	2	3	2				2	2		3	2	3	3
Outcome 4	2	2	2	2	2				3	3	2	3	3	3	3
Course Average	**2**	**3**	**2**	**3**	**2**				**2**	**2**	**1**	**3**	**2**	**3**	**3**

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References
Unit 1	**Introduction of VHDL & Logic synthesis**	**9**		
1.	Concepts of Hardware Description Languages	2	1	1,2
2.	VHDL objects, types, subtypes, operators, packages	2	1	1,2
3.	Design cycle synthesis,	1	1	1, 2
4.	Types of synthesizers, design optimization techniques	2	1	1, 2
5.	Technology mapping, design organization	2	1	1, 2
Unit 2	**Combinational Logic & Sequential logic design**	**11**		
6.	Design units, entities and architectures	2	2,4	1,2
7.	Simulation and synthesis model, signals and ports	1	2,4	1,2,3
8.	Simple signal assignments, conditional signal assignments, selected signal assignment	2	2,4	1,2,3
9.	Processes, variables, sequential statements	1	2,4	1,2,3
10.	Registers: Simulation and synthesis model of register, register templates, clock types, gated registers, resettable registers,	2	2,4	1,2,3

11.	Simulation model of asynchronous reset, asynchronous reset templates, registered variables	2	2,4	1,2,3
12.	FSM: Moore and Mealy machine modelling	1	2,4	1,2,5
Unit 3	**Hierarchy & Sub programs**	**8**	2,4	1,2,5
13.	Components, component instances, component declaration, generate statements	2	2,4	1,2,5
14.	Configuration specifications, default binding, binding process, component packages.	2	2,4	1,2,5
15.	Sub programs functions, procedures	2	2,4	1,2,5
16.	Declaring subprograms.	2	2,4	1,2,5
Unit 4	**Test Benches & Verilog**	**9**		
17.	Test benches, verifying responses	2	3,4	1,2,5
18.	Printing response values, reading data files	2	3,4	1,2,5
19.	Overview of Digital Design with Verilog HDL	1	3,4	1,2,5
20.	Basic Concepts, Modules and Ports, Basics of Gate-Level Modeling	2	3,4	1,2,5
21.	Dataflow Modeling, Behavioral Modeling.	2	3,4	1,2,5
Unit 5	**FPGA**	**8**		
22.	Introduction, Logic Block Architecture, Routing Architecture, Programmable, Interconnection,	2	1,4	1,2,5
23.	Design Flow, Xilinx Virtex-II, Artix-7 (Architecture)	2	1,4	1,2,5
24.	Boundary Scan, Programming FPGA's	2	1,4	1,2,5
25.	Interface of FPGA board with input and output devices.	2	1,4	1,2,5
	Total	**45**		

Recommended Resources

1. Charles H. Roth, Digital System Design Using VHDL , Jr.,Thomson, (2008)2nd Ed.
2. Bhaskar, J., A VHDL Primer, Pearson Education/ Prentice Hall (2006)3rd Ed.

Other Resources

3. Ashenden, P., The Designer's Guide To VHDL, Elsevier (2008) 3rd Ed.
4. David C. Black and Jack Donovan, SystemC: From the Ground Up, Springer, (2014) 2nd Ed.
5. Rushton, A., VHDL for Logic Synthesis, Wiley (1998) 2ed.
6. Samir Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, Prentice Hall PTR (2003) 2nd Ed.

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)				End Semester Exam (50%)
		CLA-1 (5%)	Mid-1 (20%)	CLA-2 (15%)	CLA-3 (10%)	
Level 1	Remember	50%	50%	40%	40%	50%
	Understand					
Level 2	Apply	45%	40%	40%	40%	40%
	Analyse					
Level 3	Evaluate	5%	10%	20%	20%	10%
	Create					
Total		**100%**	**100%**	**100%**	**100%**	**100%**

Course Designer(s)

a. ***Dr. M. Durga Prakash***. *Asst. Professor. Dept. Of ECE. SRM University – AP*

SRM University – AP, Andhra Pradesh

Neerukonda, Mangalagiri Mandal
Guntur District, Mangalagiri, Andhra Pradesh 522240

Project management

Course Code	**VLS 508**	Course Category	**Core Course (CC)**	L-T-P-C	**0**	**2**	**1**	**3**
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)				
Course Offering Department	**Mechanical Engineering**	Professional / Licensing Standards						

Course Objectives / Course Learning Rationales (CLRs)

Objective 1: To understand the fundamentals of production and operations management.

Objective 2: To learn about capacity planning, plant layout, scheduling and sequencing

Objective 3: To learn about operation management, work study, time study

Objective 4: To understand about Inventory control, supply chain management

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course students will be able to	**Bloom's Level**	**Expected Proficiency Percentage**	**Expected Attainment Percentage**
Outcome 1	Define and explain the basic concepts and principles of production and operations management (POM),	1	80%	75%
Outcome 2	Develop proficiency in capacity planning, plant layout etc.	2	70%	75%
Outcome 3	Able to perform work study, time study, gantt chart	3	80%	70%
Outcome 4	Explain supply chain management functions and applicaions	2	80%	75%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)														
	Engineering	Problem Analysis	Design and	Analysis, Design and	Modern Tool and ICT	Society and	Environment and	Moral, and Ethical	Individual and	Communication Skills	Project Management	Self-Directed and Life	PSO 1	PSO 2	PSO 3
Outcome 1	3	3	1	3	2				3			3	3	2	3
Outcome 2	3	3	2	3	2				3			3	3	2	3
Outcome 3	3	3	2	3	2				3			3	3	2	3
Outcome 4	3	3	3	3	2				3			3	3	3	3
Course Average	**3**	**3**	**2**	**3**	**2**				**3**			**3**	**3**	**2**	**3**

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
	UNIT-I Fundamental concepts	**8**	**1**	**1**
1.	Production planning and control	2	1	1
2.	New product development	1	1	1,2
	UNIT-II Plant layout	**8**		
3.	Capacity planning, facility planning	2	1	1
4.	Plant location and layout	2	1,2	1,2
5.	Scheduling and sequencing	2	1,2	1,2
	UNIT- III Operation management	**9**		
6.	CPM	3	3	1
7.	Gantt chart	3	3	2
8.	Work study, time study	3	3	1,2
	UNIT-IV- Material management	**10**		
9.	ABC analysis, EOQ	3	3,4	1

10.	Supply chain management	4	3,4	1
11.	Preventive maintenence	3	3,4	2
	UNIT – V Tools	**10**		
12.	Six sigma, Poka yoke, BPR, ERP, Kanban, ISO 9000,	5	3,4	2
13.	JIT, TQM, FMS, Push/Pull, Kaizen, CAD CAM	5	3,4	2
Total Contact hours		**45**		

Recommended Resources

1. Production and Operations Management by Bhattacharyya, Universal Press
2. Production and Operations Management by Panneer selvam R; Publisher: Prentice Hall of India

Learning Assessment

Bloom's Level of Cognitive Task		**Continuous Learning Assessments (50%)**				**End Semester Exam (50%)**
		CLA-1 (20%)	**CLA-1 (15%)**	**Midterm-1 (15%)**		
		Th.	**Th.**	**Th.**	**Th.**	**Th.**
Level 1	Remember / Understand	50%	40%	50%	45%	30%
Level 2	Apply / Analyse	50%	60%	50%	55%	70%
Level 3	Evaluate / Create					
Total		**100%**	**100%**	**100%**		**100%**

Course Designers

Prof. Prakash Jadhav, *Professor, Department of Mechanical Engineering, SRM university AP.*

SEMESTER III

SRM University – AP, Andhra Pradesh

Neerukonda, Mangalagiri Mandal

Guntur District, Mangalagiri, Andhra Pradesh 522240

Thesis I

Course Code	**VLS 509**	Course Category	**Project**	L-T-P-C	**0**	**0**	**14**	**14**
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)				
Course Offering Department	**Electronics and Communication Engineering**	Professional / Licensing Standards						

Course Objectives / Course Learning Rationales (CLRs)

Objective 1: Survey the existing research works/literature and analyze them.

Objective 2: Demonstrate the skills acquired to solve a technical problem.

Objective 3: To have a systematic approach to solve the given problem.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course, the learner will be able to	**Bloom's Level**	**Expected Proficiency Percentage**	**Expected Attainment Percentage**
Outcome 1	Review and analyze the existing research work systematically.	3	80%	70%
Outcome 2	Attain strong technical, and domain knowledge in the field of project.	3	80%	70%
Outcome 3	Formulate the complex problem and have a systematic approach for the solution.	2	80%	70%
Outcome 4	Conduct research project	2	80%	70%
Outcome 5	Communicate the technical problems with peers and mentors to move towards appropriate solutions.	2	75%	70%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	**Program Learning Outcomes (PLO)**												
	Engineering Knowledge	Conduct Investigations of Complex Problems	Design and Development	Modern Tools Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life Long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	2	2					2	2	2	1	1	3
Outcome 2	3	3	3	1			1	2	1	2	1	1	3

Outcome 3	2	3	2		1	1	1	2	1	2	1	1	3
Outcome 4	2	3	2	1	1	1	1	2	2	3	1	1	3
Outcome 5	2	3	2		1	1	1	2	3	3	1	1	3
Course Average	**2**	**3**	**2**	**1**	**1**	**1**	**1**	**2**	**2**	**2**	**1**	**1**	**3**

Course Unitization Plan

The student is expected to spend a minimum of 12 hours/week on the Project work.

Learning Assessment

Bloom's Level of Cognitive Task		**Continuous Learning Assessments (50%)**				**End Semester Exam (50%)**	
		Review -I		**Mid Review**		**Final Review**	
		Th	**Prac**	**Th**	**Prac**	**Th**	**Prac**
Level 1	Remember		20%		20%		20%
	Understand						
Level 2	Apply		80%		80%		80%
	Analyse						
Level 3	Evaluate						
	Create						
Total			100%		100%		100%

Course Designers

Dr. Dutgaprakash M, Department of Electronics and Communication Engineering, SRM University - AP

SEMESTER IV

SRM University – AP, Andhra Pradesh
Neerukonda, Mangalagiri Mandal
DrDrGuntur District, Mangalagiri, Andhra Pradesh 522240

Thesis II

Course Code	**VLS 511**	Course Category	**Project**	L-T-P-C	**0**	**0**	**15**	**15**
Pre-Requisite Course(s)		Co-Requisite Course(s)		Progressive Course(s)				
Course Offering Department	**Electronics and Communication Engineering**	Professional / Licensing Standards						

Course Objectives / Course Learning Rationales (CLRs)

Objective 1: Survey the existing research works/literature and analyse them.

Objective 2: Demonstrate the skills acquired to solve a technical problem.

Objective 3: To have systematic approach to solve the given problem.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course, the learner will be able to	**Bloom's Level**	**Expected Proficiency Percentage**	**Expected Attainment Percentage**
Outcome 1	Review and analyse the existing research work in a systematic way.	3	80%	70%
Outcome 2	Attain strong technical, domain knowledge in the field of project.	3	80%	70%
Outcome 3	Formulate the complex problem and to have systematic approach for the solution.	2	80%	70%
Outcome 4	Conduct research project	2	80%	70%
Outcome 5	Communicate the technical problems with peers and mentors to move towards appropriate solution.	2	75%	70%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	**Program Learning Outcomes (PLO)**												
	Engineering Knowledge	Conduct Investigations of Complex Problems	Design and Development	Modern Tools Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Teamwork Skills	Communication Skills	Life Long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	2	2					2	2	2	1	1	3
Outcome 2	3	3	3	1			1	2	1	2	1	1	3
Outcome 3	2	3	2		1	1	1	2	1	2	1	1	3

Outcome 4	2	3	2	1	1	1	1	2	2	3	1	1	3
Outcome 5	2	3	2		1	1	1	2	3	3	1	1	3
Course Average	**2**	**3**	**2**	**1**	**1**	**1**	**1**	**2**	**2**	**2**	**1**	**1**	**3**

Course Unitization Plan

The student is expected to spend at least 32 hours/week on the Project work.

Learning Assessment

Bloom's Level of Cognitive Task		**Continuous Learning Assessments (50%)**				**End Semester Exam (50%)**	
		Review -I		**Mid Review**		**Final Review**	
		Th	**Prac**	**Th**	**Prac**	**Th**	**Prac**
Level 1	Remember		20%		20%		20%
	Understand						
Level 2	Apply		80%		80%		80%
	Analyse						
Level 3	Evaluate						
	Create						
Total			100%		100%		100%

Course Designers

Dr. Durga Prakash M, Department of Electronics and Communication Engineering, SRM University - AP

ELECTIVES

SRM University – AP, Andhra Pradesh

Neerukonda, Mangalagiri Mandal
Guntur District, Mangalagiri, Andhra Pradesh 522240

Sensor Technology and MEMS

Course Code	**VLS562**	Course Category	**Specialty Stream Courses (C)**	L-T-P-C	**3**	**0**	**0**	**3**
Pre-Requisite Course(s)	**VLS513**	Co-Requisite Course(s)	**Nil**	Progressive Course(s)				
Course Offering Department	**ECE**	Professional / Licensing Standards						
Board of Studies Approval Date		Academic Council Approval Date						

Course Objectives / Course Learning Rationales (CLRs)

Objective 1: To understand MEMS and microfabrication

Objective 2: To study the essential material properties.
Objective 3: To study various sensing and transduction technique.
Objective 4: To know various fabrication and machining process of MEMS
Objective 5: To know about the polymer and optical MEMS.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	**Bloom's Level**	**Expected Proficiency Percentage**	**Expected Attainment Percentage**
Outcome 1	Be familiar with the important concepts applicable to MEMS and their fabrication	2	70%	65%
Outcome 2	Discuss the design, analysis and testing of MEMS required material properties	2	70%	65%
Outcome 3	Discuss the various sensing and transduction techniques	3	70%	65%
Outcome 4	Discuss various fabrication and machining process of MEMS	3	70%	65%
Outcome 5	Illustrate the applications of the polymer and optical MEMS devices	4	70%	65%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Design / Development of Solutions Conduct Investigations of Complex Problems	Conduct Investigations of Complex Problems	Modern Tool Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Team Work	Communication	Life-long Learning	PSO1	PSO2	PSO3
Outcome 1	1	2	1	3	2	3	2	2	2	3	3	2	2
Outcome 2	1	2	2	3	2	1	2	2	3	3	2	3	2
Outcome 3	1	2	2	3	2	1	2	2	3	2	3	3	2
Outcome 4	1	2	2	3	2	3	3	3	3	3	3	3	3
Outcome 5	2	3	2	3									
Outcome 6	2	2	2	3									
Course Average	2	2	1	3	2	2	2	2	3	3	3	3	2

Course Unitization Plan- Theory

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit I	**Introduction to Microfabrication**	**10**		
1.	Review of Photolithography	2	1	1,3
1.	Thin Film Deposition, Thermal Oxidation of Silicon	2	1	1,3
1.	Wet Etching, Silicon Anisotropic Etching, Plasma Etching and Reactive Ion Etching	2	2	1,3

1.	Doping	1	3	1,3
1.	Wafer Dicing, Wafer Bonding	1	2	1,3
1.	Packaging and Integration	1	2	1,3
1.	Surface Micromachining	1	2	1,3
Unit II	**Electrical and Mechanical Concepts**	10		
1.	Conductivity of Semiconductor	1	1	1,2
1.	Crystal Planes and Orientations	2	1	1,2
1.	Stress and Strain	1	2	1,2
1.	Flexural Beam Bending Analysis Under Simple Loading Conditions	2	3	1,2
1.	Intrinsic Stress, Dynamic System	2	2	1,2
1.	Resonant Frequency, and Quality Factor	2	2	1,2
Unit III	**Electrostatic and Thermal Sensing and Actuation**	**8**		
16.	Parallel-Plate Capacitor, Applications of Parallel-Plate Capacitors (Inertia Sensor, Pressure Sensor, Flow Sensor, Tactile Sensor, Parallel-Plate Actuators)	2	2	2,3
17.	Interdigitated Finger Capacitors, Applications of Comb-Drive Device (Inertia Sensors, Actuators)	2	2	2,3
18.	Thermal Sensors and Actuators, Fundamentals of Thermal Transfer, Sensors and Actuators Based on Thermal Expansion	2	2	2,3
19.	Thermocouple and Thermal resistors, Applications (Inertia Sensors, Flow sensors, Infrared sensors)	2	2	2,3
Unit IV	**Piezoresistive Sensors and Piezoelectric Sensing and Actuation**	**9**		
23.	Expression of Piezoresistivity, Piezoresistive Sensor Material (Single Crystal Silicon, Polycrystalline Silicon)	2	3	1,2
24.	Stress Analysis of Mechanical Elements, Applications of Piezoresistive Sensors (Inertia Sensor, Pressure Sensor, Flow Sensor, Tactile Sensor);	4	3	1,2
25.	Mathematical Description of Piezoelectric Effects, Properties of Piezoelectric Materials, Applications (Inertia Sensor, Acoustic, Flow Sensor, Tactile Sensor).	4	3	1,2
Unit V	**Polymer MEMS, Microfluidics and Case Studies**	**8**		
32.	Polymers in MEMS, Applications of polymers	2	4	2,3
33.	Fluid Mechanics Concepts, Microfluidic channels and valves	2	4	2,3
34.	Case studies (Capacitive accelerometer, Piezoelectric Gyroscope)	2	4	2,3
35.	Case studies (DNA amplification, Microbridge gas sensor)	2	4	2,3
Total Contact Hours		**45**		

Recommended Resources

1. S.M.Sze, “VLSI Technology”, McGraw Hill, 2nd Edition. 2008
2. Chang Liu, “Foundations of MEMS” Prentice Hall, 2012
3.S D Senturia, “MICROSYSTEM DESIGN”, Kluwer Academic Publishers, 2002.

Learning Assessment

Bloom’s Level of Cognitive Task		Continuous Learning Assessments (50%)				End Semester Exam (50%)
		Theory (30%)				
		CLA-1 (5%)	Mid-1 (10%)	CLA-2 (5%)	Mid-2 (10%)	Th
Level 1	Remember	60%	40%	60%	40%	30%
	Understand					
Level 2	Apply	40%	60%	40%	60%	70%
	Analyse					
Level 3	Evaluate					
	Create					
Total		**100%**	**100%**	**100%**	**100%**	**100%**

Course Designers

a. Dr. M. Durga Prakash, Assistant Professor, Department of ECE, SRM University – AP

Course Code	TE-1	**Course Category**	CE	**L-T-P-C**	3	0	0	3
Pre-Requisite Course(s)		**Co-Requisite Course(s)**		**Progressive Course(s)**				
Course Offering Department	ECE	**Professional / Licensing Standards**	*IEEE, Microsoft, Cadence, Vivado*					

Course Objectives / Course Learning Rationales (CLRs)

Objective 1: To study the various CAD tools and methodologies employed in the design of VLSI circuits.

Objective 2: To understand the RTL (Register-Transfer Level) design, logic synthesis, physical design, and simulation.

Objective 3: To learn design and testing of VLSI circuits using CAD tools.

Objective 4: To evaluate and enhance the performance of VLSI designs through CAD tools.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	**Bloom's Level**	**Expected Proficiency Percentage**	**Expected Attainment Percentage**
Outcome 1	Learn industry-standard CAD tools, navigating schematic capture, layout design, and verification tools for VLSI circuits.	2	80%	70%
Outcome 2	Apply theoretical concepts into practical applications.	3	70%	60%
Outcome 3	Analyse, identify bottlenecks, optimize VLSI designs for Performance, Power, and Area (PPA) using CAD tools.	4	80%	70%
Outcome 4	Exhibit adaptability to evolving CAD technologies, ensuring they stay current with advancements in the dynamic field of VLSI design.	4	70%	60%

Course Articulation Matrix: (CLO) to Program Learning Outcomes (PLO)

	Program Learning Outcomes (PLO)

CLOs	Engineering Knowledge	Problem Analysis	Design and Development	Analysis, Design and Research	Modern Tool and ICT Usage	Society and Multicultural Skills	Environment and Sustainability	Moral, and Ethical Awareness	Individual and Teamwork Skills	Communication Skills	Project Management and Finance	Self-Directed and Life Long Learning	PSO1	PSO2	PSO3
Outcome 1	3	2	1	2					2		1			1	2
Outcome 2	3	3	2	2					3				1	3	2
Outcome 3	3	3	3	3					2				1	3	3
Outcome 4	3	3	3	3					3		3		1	3	3
Course Average	**3**	**3**	**3**	**3**					**3**		**1**		**1**	**3**	**3**

Course Unitization Plan -Theory

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References
Unit 1	**Introduction to VLSI Design and CAD Tools**	**9**		

	Understand the stages of the VLSI design process, from conceptualization to fabrication.	1	1	1,2
	Trace the historical development of VLSI technology and its impact on computing.	1	1	1,2
	Examine key milestones and breakthroughs that shaped the VLSI landscape.	1	1	1,2
	Analyze the pivotal role of Computer-Aided Design (CAD) tools in VLSI design.	1	1,2	1,2
	Discuss how CAD tools enhance efficiency, accuracy, and productivity in VLSI workflows.	1	1,2	1,2
	Explore Electronic Design Automation (EDA) tools and their roles in the design flow.	1	1,2	1,2

	Discuss the impact of CAD tools on reducing time-to-market and overall design cost.	1	1,2	1,2
	Introduce students to a basic CAD tool interface.	1	1,2	1,2,4,6
	Conduct introductory exercises to familiarize students with basic CAD operations.	1	1,2	1,2,4,6
Unit 2	**Digital Design Fundamentals**	**9**		
	Apply Boolean algebra to simplify and manipulate logical expressions.	1	2,3	1,2
	Design and analyze combinational circuits using logic gates.	1	2,3	1,2
	Introduce sequential circuits, including flip-flops and latches.	1	1,2,3	1,2
	Discuss the concept of clocking and its importance in sequential circuit design.	1	1,2,3	1,2
	Define Register-Transfer Level (RTL) design and its role in VLSI.	1	1,2,3	1,2
	Demonstrate the translation of high-level design concepts into RTL descriptions.	1	1,2,3	1,2
	Engage students in practical RTL design exercises.	1	2,3	1,2
	Implement simple digital circuits using RTL design principles.	1	2,3	1,2
	Utilize simulation tools to validate the functionality of RTL designs.	1	2,3	1,2
Unit 3	**Schematic Capture and Simulation Tools**	**9**		

	Introduce functional simulation using Verilog or VHDL.	1	2,3,4	1,2,3
	Create and simulate basic digital circuits to understand functional behavior.	1	2,3,4	1,2,3
	Optimize circuit designs for better performance using timing constraints	1	2,3,4	1,2,3
	Apply simulation tools to analyze and troubleshoot real-world digital circuits.	1	2,3,4	1,2,3
	Discuss the significance of simulation in identifying design flaws.	1	2,3,4	1,2,3
	Introduce advanced simulation techniques such as mixed-signal simulation.	1	2,3	1,2,3
	Explore co-simulation of analog and digital components.	1	2,3,4	1,2,3
	Conduct hands-on sessions for students to create and simulate circuits using schematic capture tools.	1	2,3,4	1,2,3
	Emphasize the practical application of simulation results in design refinement.	1	2,3	1,2,3
Unit 4	**Logic Synthesis and Optimization Techniques**	**9**		
	Define logic synthesis and its role in transforming RTL descriptions into gate-level netlists.	1	2,3,4	1,2,5
	Discuss strategies for optimizing designs in terms of area, power, and performance (PPA).	1	2,3,4	1,2,5
	Introduce technology mapping as a critical step in the synthesis process.	1	2,3,4	1,2,5
	Cover advanced logic synthesis techniques, including retiming and resynthesis.	1	2,3,4	1,2,5
	Explore the impact of these techniques on design quality and efficiency.	1	2,3,4	1,2,5
	Demonstrate the application of logic synthesis techniques through practical examples.	1	2,3,4	1,2,5
	Guide students in optimizing designs for specific criteria.	1	2,3,4	1,2,5
	Discuss current challenges in logic synthesis.	1	2,3,4	1,2,5
	Explore emerging trends and future directions in logic synthesis research and development.	1	2,3,4	1,2,5
Unit 5	**Physical Design and Layout**	**9**		
	Provide an overview of the physical design process, from initial floor planning to tape-out.	1	3,4,5	1,2,5
	Introduce floor planning as a critical step in physical design.	1	2,3,4	1,2,5
	Explain the global and detailed routing stages in the physical design flow.	1	2,3,4	1,2,5
	Discuss algorithms and techniques for efficient and effective routing.	1	3,4,5	1,2,5
	Cover the significance of physical verification in ensuring design correctness.	1	2,3,4	1,2,5
	Introduce Design Rule Checking (DRC) and its role in identifying layout violations.	1	2,3,4	1,2,5
	Conduct hands-on sessions for students to implement physical design principles.	1	3,4,5	1,2,5

	Guide students through the process of floorplanning, placement, and routing.	1	2,3,4	1,2,5
	Discuss advanced topics such as clock tree synthesis and power planning.	1	2,3,4	1,2,5
	Total	**45**		

Learning Assessment (Integrated course)

Bloom's Level of Cognitive Task		**Continuous Learning Assessments (50%)**				**End Semester Exam (50%)**
		CLA-1 (10%)	**Mid-1 (15%)**	**CLA-2 (10%)**	**Mid-2 (15%)**	
Level 1	Remember	80%	50%	20%	20%	20%
	Understand					
Level 2	Apply	20%	50%	80%	80%	80%
	Analyse					
Level 3	Evaluate					
	Create					
Total		**100%**	**100%**	**100%**	**100%**	**100%**

Course Designer(s)

Dr. Pradyut Kumar Sanki, Associate Professor, Dept. of ECE, SRM University – *AP*

More Than Moore's Electronics

Course Code	VLS 580	**Course Category**	Departmental Core Elective	**L-T-P-C**	3	0	0	3

Pre-Requisite Course(s)	VLSI Technology	**Co-Requisite Course(s)**		**Progressive Course(s)**	
Course Offering Department	ECE	**Professional / Licensing Standards**	*IEEE, Microsoft, Cadence*		

Course Objectives / Course Learning Rationales (CLRs)

Objective 1: To explore the limitations and challenges associated with traditional Moore's Law scaling and delve into alternative approaches for improving electronic devices.

Objective 2: To study and analyze emerging technologies that contribute to electronic advancements, such as 3D integration, heterogeneous integration, and new materials.

Objective 3: To gain proficiency in designing electronic systems with an emphasis on energy efficiency, thermal management, and overall system efficiency by taking into account power optimization.

Objective 4: Recognize the interdisciplinary nature of More than Moore's Electronics by exploring contributions from fields such as materials science, physics, and engineering.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course, the learner will be able to	**Bloom's Level**	**Expected Proficiency Percentage**	**Expected Attainment Percentage**
Outcome 1	Understand the limitations and challenges associated with traditional Moore's Law scaling and delve into alternative approaches for improving electronic devices	3	80%	75%
Outcome 2	Understand and analyze the emerging technologies that contribute to electronic advancements, such as 3D integration, heterogeneous integration, and new materials	4	85%	80%
Outcome 3	Design electronic systems with an emphasis on energy efficiency, thermal management, and overall system efficiency	6	80%	75%
Outcome 4	Understand the interdisciplinary nature of More than Moore's Electronics and strongly motivated towards integration of materials science, physics, and engineering research into designing future 3D-IC systems.	5	85%	75%

Course Articulation Matrix: (CLO) to Program Learning Outcomes (PLO)

	Program Learning Outcomes (PLO)

CLOs	Engineering Knowledge	Design / Development of Solutions Conduct Investigations of Complex Problems	Conduct Investigations of Complex Problems	Modern Tool Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Team Work	Communication	Life-long Learning	PSO1	PSO2	PSO3
Outcome 1	**2**	**3**	**2**	**2**	**2**	**2**	**2**	**3**	**3**	**3**	**3**	**2**	**1**
Outcome 2	**3**	**3**	**2**	**2**	**2**	**1**	**2**	**2**	**2**	**3**	**3**	**3**	**2**
Outcome 3	**3**	**3**	**2**	**3**	**2**	**1**	**2**	**3**	**2**	**3**	**3**	**3**	**3**
Outcome 4	**3**	**2**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**3**	**3**	**3**
Course Average	**3**	**3**	**2**	**2**	**2**	**2**	**2**	**3**	**2**	**3**	**3**	**3**	**2**

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
UNIT I	**Introduction to 3D-IC technology**	**14**		
	Introduction to Moore's Law and MOSFET Technology	2	1	1,2,3
	Scaling Theory	2	1	1,2,3

	Evolution of MOSFET	5	1	1,2,3
	Requirements to go beyond Moore's Law	2	1	1,2,3
	Transistor scaling & Research roadmap	2	1	1,2,3
	CMOS feature directions	1	1	1,2,3
Unit II	**3D-Interconnects**	**6**		
	Classification and advantages of 3-D Integration	1	2,4	1,2,3
	Interconnects scaling theory and performance evolution,	2	2,4	1,2,3
	3D Interconnects	1	2,4	1,2,3
	On-chip device (vs) Interconnected device	1	2,4	1,2,3
	3D device (vs) Multicore device.	1	2,4	1,2,3
Unit III	**3D-Bonding**	**16**	2,4	
	Interconnect Technology & Classification of Interconnects	1	2,4	1,2,3
	Blanket and Non-Blanket bonding	2	2,4	1,2,3
	Direct bonding and Thermo-Compression bonding	3	2,4	1,2,3
	Passivated and Un-passivated bonding	2	2,4	1,2,3
	Metallic, Dielectric and Hybrid bonding	2	2,4	1,2,3
	Bond quality characterization techniques	2	2,4	1,2,3
	Grand challenges in bonding technology	1	2,4	1,2,3
	Wafer orientation strategies in 3D stacks	2	2,4	1,2,3
	Daisy Chain	1	2,4	1,2,3
UNIT IV	**Through-Silicon-Via (TSV)**	**6**		
	TSV Classification and Fabrication methods	1	3,4	1,2,3
	TSV Integration strategies	1	3,4	1,2,3
	TSV Cooling strategies	1	3,4	1,2,3
	TSV Electrical & Thermal modelling	2	3,4	1,2,3
	TSV Testing	1	3,4	1,2,3
UNIT V	**Other Si Electronics**			

		7		
	Spintronics, Spin FET	2	4	4
	Magnetic Tunnel Junction, Spin Transistors	2	4	4
	Organic Electronics, Organic Light Emitting Diodes (OLED), Organic Thin Film Transistors (OTFT)	2	4	4
	Organic Photovoltaic Cells (OPC)	1	4	4
Total Contact Hours		**49**		

Recommended Resources

1. Handbook Of 3D Integration: Volumes 1 And 2: Technology And Applications Of 3D Integrated Circuits by Gorrou, John Wiley.
2. 3D IC Integration and Packaging by John H. Lau.
3. Silicon VLSI Technology: Fundamentals, Practice and Modelling by James D. Plummer, Michael D. Deal, Peter B. Griffin.
4. Organic Electronics: Materials, Processing, Devices and Applications by Franky So.

Other Resources

1. Weste, N.H.E., Harris, D. and Banerjee, A., CMOS VLSI Design, Dorling Kindersley (2006) 3rd ed..

Learning Assessment (Theory)

Bloom's Level of Cognitive Task		**Continuous Learning Assessments (60%)**				**End Semester Exam (40%)**
		CLA-1 (15%)	**Mid-1 (15%)**	**CLA-2 (15%)**	**CLA-3 (15%)**	
Level 1	Remember	50%	45%	30%	50%	40%
	Understand					
Level 2	Apply	40%	50%	50%	40%	50%
	Analyse					

Level 3	Evaluate	10%	5%	20%	10%	10%
	Create					
Total		**100%**	**100%**	**100%**	**100%**	**100%**

Course Designer(s)

a. ***Dr. Patta Supraja****. Asst. Professor. Dept. Of ECE. SRM University – AP*

With reference to ***Dr***. ***Shiv Govind Singh****, Professor, Dept. Of EE. IIT Hyderabad*.

VLSI Physical Design

Course Code	VLS 481	**Course Category**	Technical Elective	**L-T-P-C**	3	0	0	3
Pre-Requisite Course(s)	VLSI Design	**Co-Requisite Course(s)**		**Progressive Course(s)**				
Course Offering Department	ECE	**Professional / Licensing Standards**						

Course Objectives / Course Learning Rationales (CLRs)

Objective 1: To understand the requirements of VLSI automation Tools.
Objective 2: To understand the requirements Proper placement and Routing of Circuits.
Objective 3: To familiarize with methods and algorithms for efficient Floor Planning and Routing
Objective 4: To understand different circuit level techniques for logic synthesis.

Objective 5: To understand how high-level synthesis is carried out for proper allocation, scheduling and assignment.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Describe various VLSI Automation Tools	2	70%	65%
Outcome 2	Implement ideas on Placement and Partitioning of Circuits	3	70%	65%
Outcome 3	Identify concepts and Algorithms of Floor planning and Routing	3	70%	65%
Outcome 4	Develop circuit level techniques and apply in logic Synthesis	3	70%	65%
Outcome 5	Working on High Level Synthesis of Circuits	4	70%	65%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)													
	Engineering Knowledge	Problem Analysis	Design and Development	Analysis, Design and Research	Modern Tool and ICT Usage	Society and Multicultural Skills	Environment and Sustainability	Moral, and Ethical Awareness	Individual and Team work Skills	Communication Skills	Project Management and Finance	Self-Directed and Life Long Learning	PSO1	PSO2	PSO3
Outcome 1	3	3	3	2	1		2					3	3	1	2
Outcome 2	3	3	3	2	2	1	2		3			2	3	2	2
Outcome 3	3	3	3	2	2		2		3			3	3	2	2
Outcome 4	3	3	3	3	2	1	2		3			2	3	2	2
Outcome 5	3	3	3	2	2	1	2		2			2	3	2	2
Course Average	**3**	**3**	**3**	**2**	**2**	**1**	**2**		**3**			**2**	**3**	**2**	**2**

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit 1	**VLSI DESIGN AUTOMATION TOOLS**	**16**		

	Algorithms and system design, Structural and logic design	2	1	1
	Transistor level design, Layout design	2	1	1
	Verification methods	1	1	1
	Design management tools	1	1	1
	Layout compaction	2	2	1
	placement and routing, Pin Assignment	2	2	1
	Design rules, symbolic layout, Applications of compaction	2	2	2
	Formulation methods, Algorithms for constrained graph compaction	2	2	2
	Circuit representation, Wire length estimation, Placement algorithms, Partitioning algorithms	2	2	2
Unit 3	**FLOOR PLANNING AND ROUTING**	**10**		
	Floor planning concepts	2	3	1,2
	Shape functions and floor planning sizing	2	3	1,2
	Local routing, Area routing	2	3	1,2
	Channel routing	2	3	1,2
	Global routing and its algorithms.	2	3	1,2
Unit 4	**SIMULATION AND LOGIC SYNTHESIS**	**10**		
	Gate level and switch level modelling and simulation	1	4	2,3
	Introduction to combinational logic synthesis	1	4	2,3
	STA	2	4	2,3
	ROBDD principles, Implementation, construction and manipulation	2	4	2,3
	Two level logic synthesis.	2	4	3,4
	Timing Closure	2	4	3,4
Unit 5	**HIGH-LEVEL SYNTHESIS**	**11**		
	Hardware model for high level synthesis	2	5	3,4
	Internal representation of input algorithms	1	5	3,4

	Allocation, assignment, and scheduling	2	5	3,4
	Scheduling algorithms, Aspects of assignment	1	5	3,4
	High level transformations	1	5	3,4

Recommended Resources

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley ,1998.
2. N.A.Sherwani , "Algorithms for VLSI Physical Design Automation", (3/e), Kluwer,1999..
3. S.M. Sait , H. Youssef, "VLSI Physical Design Automation", World scientific, 1999
4. cadence.com/content/dam/cadence-www/global/en_US/documents/tools/digital-design-signoff/innovus-implementation-system-ds.pdf

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (60%)								End Semester Exam (40%)	
		CLA-1 (15%)		Mid-1 (15%)		CLA-2 (15%)		Mid-2 (15%)			
		Th		Th		Th		Th		Th	
Level 1	Remember	60%		50%		60%		50%		40%	
	Understand										
Level 2	Apply	40%		50%		40%		50%		60%	
	Analyze										
Level 3	Evaluate										
	Create										
Total		**100%**		**100%**		**100%**		**100%**		**100%**	

Course Designers

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Advanced CMOS Digital IC Design

Course Code	VLS 482	**Course Category**	Elective	**L-T-P-C**	3	0	0	3
Pre-Requisite Course(s)		**Co-Requisite Course(s)**	TEC	**Progressive Course(s)**				
Course Offering Department	ECE	**Professional / Licensing Standards**						

Course Objectives

1. To study advanced concepts of CMOS Digital Design. It will be helpful for the students when they work in VLSI industries or R&D's.
2. To cover crucial real world system design issues such as signal integrity, power dissipation, interconnect packaging, timing and synchronization.
3. To provide unique coverage of the latest design methodologies and tools.
4. To learn Low-power design concepts and voltage-frequency scaling.

Course Outcome (COs)

CO's	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
1	To understand the fundamental principles of CMOS technology, including the operation of MOS transistors, logic gates, and basic building blocks.	2	75%	65%
2	Modelling and estimation of R, C, and L parasitic, effect of technology scaling, sheet resistance, techniques to cope with ohmic drop and capacitive cross talk, estimating RC delay, and inductive effects.	1	75%	65%
3	Several lab team assignments to design actual VLSI subsystems from high-level specifications, culminating in a course project involving the software design of a modest complexity chip.	3	75%	65%
4	Several homework assignments based on core concepts and reinforcing analytical skills learned in class.	3	75%	65%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)														
	Engineering Knowledge	Problem	Design and Development	Analysis, Design and	Modern Tool and ICT	Society and Multicultural	Environment and	Moral, and Ethical	Individual and Teamwork	Communication Skills	Project Management	Self-Directed and Life Long	PSO 1	PSO 2	PSO 3
Outcome 1	3	2	3	3	2	-	-	-	-	-	3	3	2	1	2
Outcome 2	3	3	3	3	2	3	1	-	3	2	3	3	3	3	3
Outcome 3	3	2	1	1	1	-	-	-	1	-	2	3	1	1	1
Outcome 4	3	2	1	2	2	-	-	-	1	-	2	3	1	1	3
Course Average	**3**	**2**	**3**	**2**	**2**	**3**	**1**	**-**	**3**	**2**	**3**	**3**	**2**	**2**	**3**

Course Unitization Plan

Unit No.	Syllabus Topics	Required Contact Hours	CLOs Addressed	References Used
Unit No. 1	**INTRODUCTION, THE WIRE, COPING WITH INTERCONNECT**	**9**		
	Impact of Interconnect Parasitic	2	1,2	1,2
	Impact of Resistance,	2	1	1
	Impact of Capacitance, Crosstalk	2	1,2	1
	Reducing RC-delay	1	1	1
	Dealing with inductance	2	1,2	1,3
	DESIGNING SEQUENTIAL LOGIC CIRCUITS	**12**		

Unit No. 2	Self-Timed Circuit Design, Self-Timed Signaling, Muller-C Element, Two Phase Handshake Protocol, Self-Resetting CMOS, Synchronizer	2	1	1,2,3
	Designing Latch and Edge triggered Register using different approaches, Clock Overlaps, C2MOS Logic, TSPC Logic	2	1,2	2,3
	Specialized edge-triggered TSPCR	2	1,2	1
	Pulse Registers, Pipelining	2	1,2	1,3
	Designing Schmitt Trigger and multi-vibrators,	2	1,2	2,3
	Design Techniques for large Fan in, Sizing combinational circuits for minimum delay,	2	3	1,2
Unit No. 3	**RATIOED LOGIC**	**6**		
	DCVSL	2	1	1,2,3
	Pass transistor Logic	2	1,2	2,3
	Differential Pass Transistor Logic	2	1,2	1
Unit No. 4	**ARITHMETIC CIRCUITS**	**9**		
	Adders- Ripple-Carry Adder, Complimentary Static CMOS FullAdder,	1	1,2	3,4
	Mirror Adder, Transmission Gate Full Adder	1	1	4
	Carry-Bypass Adder, Carry-Select Adder	2	1	4
	Logarithmic Look-Ahead Adder, Tree Adders	2	1,2	4
	Multipliers (Array Multiplier, Wallace-Tree Multiplier, Booths Multiplier Algo)	2	1,2	3,4
	Shifters (Barrel Shifter, Logarithmic Shifter).	1	3	3,4
Unit No. 5	**SEMICONDUCTOR MEMORIES**	**9**		
	Memory Timing, Memory Architecture, Read-Only Memory Cells	1	4	1,5
	MOS OR ROM, MOS NOR ROM, MOS NAND ROM	2	4	2,5
	Dual Data rate Synchronous Dynamic RAM	2	4	5
	DRAM Timing, Sources of Power Dissipation in Memories, Data Retention in SRAM	2	4	5
	Suppressing Leakage in SRAM, Data Retention in DRAM	2	4	3,5

Recommended Resources

1. J. Rabaey, A. Chandrakasan and Nikolic, B., Digital Integrated Circuits – A Design perspective, Pearson Education (2007) 2nd ed.

2. John P. Uyemura; "Introduction to VLSI Circuits and Systems", John Wiley & Sons, Inc, 2002.

3. Kang, S. and Leblebici, Y., CMOS Digital Integrated Circuits – Analysis and Design, Tata McGraw Hill

4. Weste, N.H.E. and Eshraghian, K., CMOS VLSI Design: A Circuits and Systems Perspective, eddision Wesley (1998) 2nd ed.

5. Baker, R.J., Lee, H. W. and Boyce, D. E., CMOS Circuit Design, Layout and Simulation, Wiley - IEEE Press (2004) 2nd ed.

Web Resources

1. URL1:- http://nptel.ac.in/courses/117106092/
2. URL2:- http://nptel.ac.in/courses/117106093/

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (60 %)								End Semester Exam (40 %)	
		CLA-1 (10 %)		CLA-2 (10 %)		CLA-3 (10 %)		Mid Term (30 %)			
		Th	Prac	Th	Prac	Th	Prac	Th	Prac	Th	Prac
Level 1	Remember	60%		60%		60%		50%		50%	
	Understand										
Level 2	Apply	30%		30%		30%		30%		30%	
	Analyse										
Level 3	Evaluate	10%		10%		10%		20%		20%	
	Create										
Total		100%		100%		100%		100%		100%	

Course Designer(s)

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CMOS RFIC Design

Course Code	VLS 483	Course Category	CC	L-T-P-C	3	0	0	3
Pre-Requisite Course(s)		Co-Requisite Course(s)	VLSI Analog IC Design	Progressive Course(s)				
Course Offering Department	ECE	Professional / Licensing Standards						

Course Objectives / Course Learning Rationales (CLRs)

Objective 1: To understand the fundamentals of RFIC design and its applications in wireless communication systems.

Objective 2: To learn CMOS technology basics and its suitability for RF applications.

Objective 3: To gain proficiency in designing and optimizing RF building blocks such as amplifiers, mixers, oscillators, and filters.

Objective 4: To develop skills in simulation and verification of RFIC designs using CAD tools.

Objective 5: To explore advanced topics in RFIC design, including noise analysis, linearity, and power management.

Objective 6: To Apply design methodologies to achieve desired specifications for wireless transceivers.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course, the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Understand the fundamental of analog IC Design, including the single-stage amplifiers and Differential Amplifiers	1,2	85%	80%
Outcome 2	Design operational amplifiers and performance of various Op-Amp topologies	3	80%	75%
Outcome 3	Create layout designs for operational amplifier circuits and understand the stability in feedback system and noise performance	3	85%	70%
Outcome 4	Apply theoretical knowledge to real-world analog and digital converter IC design projects	3	80%	70%
Outcome 5	Explore emerging trends in RFIC design including mm-wave and high-frequency applications.	3	80%	70%
Outcome 6	Collaborate in teams to solve design challenges and implement solutions in RFIC design projects.	3	80%	70%

Course Articulation Matrix: (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)

	Engineering Knowledge	Design / Development of	Conduct Investigations of	Modern Tool Usage	The Engineer and Society	Environment and Sustainability	Ethics	Individual and Team Work	Communication	Life-long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	2	2	2	2	--	--	--	--	3	3	2	2
Outcome 2	3	3	3	2	2	--	--	--	--	3	2	3	2
Outcome 3	3	3	3	3	2	--	--	2	--	2	3	3	2
Outcome 4	3	3	3	3	2	--	--	3	--	3	3	3	3
Outcome 5													
Outcome 6													
Course Average	**3.00**	**2.75**	**2.75**	**2.50**	**2.00**	**--**	**--**	**1.25**	**--**	**2.75**	**2.75**	**2.75**	**2.25**

Course Unitization Plan -Theory

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References
Unit 1	**Introduction to RFIC Design**	**10**		
	Overview of RF systems and applications	2	1	1,2
	Challenges in RFIC design and performance metrics	2	1	1,2
	CMOS Technology Basics for RFICs	2	1	1,2
	Overview of CMOS process technology	2	1	1,2
	Impact of technology scaling on RF performance	2	1,3	1,2
Unit 2	**RFIC Building Blocks and Passive RF Components**	**9**		
	Low Noise Amplifiers (LNAs)	1	1	1,2
	Mixers and frequency synthesizers	2	1	1,2
	Power amplifiers (PAs) and modulators	2	1	1,2
	Inductors, capacitors, and transmission lines in CMOS	2	1	1,2
	Modeling and layout considerations for passive components	2	2,3	1,2
Unit 3	**RFIC Design Methodologies, Simulation and Characterization**	**9**		
	Design specifications and trade-offs	1	2	1,2
	Transistor-level design techniques (e.g., cascode, current mirrors)	2	1,2	1,2
	CAD tools for RFIC design (e.g., ADS, Cadence Virtuoso)	3	2	1,2
	Noise analysis, linearity, and stability analysis	3	2	1,2
Unit 4	**Advanced RFIC Design, Testing and Validation**	**9**		
	Frequency planning and synthesis	1	1	1,2
	Phase-locked loops (PLLs) and clock generation circuits	2	1,2	1,2
	Nonlinear distortion and intermodulation analysis	2	2	1,2,3
	Test methodologies and measurement techniques	2	2,3	1,2,3
	Yield analysis and reliability considerations	2	3	1,2,3
Unit 5	**Case Studies and Applications**	**8**		
	Design examples of RF front-end circuits (e.g., for wireless communication standards)	4	3,4	2,3

	Emerging trends in RFIC design (e.g., IoT, mm-wave applications)	4	3,4	2,3
	Total	**45**		

Recommended Texts and References

1. Razavi, B., & Behzad, R. (2012). RF microelectronics (Vol. 2, pp. 255-333). New York: Prentice hall.
2. Yuan, J. S. (2016). CMOS RF Circuit Design for Reliability and Variability. Springer.
3. Research papers and application notes from semiconductor manufacturers

Learning Assessment

Bloom's Level of Cognitive Task		Continuous Learning Assessments (50%)				End Semester Exam (50%)
		CLA-1 (10%)	Mid-1 (15%)	CLA-2 (15%)	CLA-3 (10%)	
Level 1	Remember	60%	50%	--	50%	40%
	Understand					
Level 2	Apply	40%	50%	60%	30%	40%
	Analyse					
Level 3	Evaluate	--	--	40%	20%	20%
	Create					
Total		**100%**	**100%**	**100%**	**100%**	**100%**

Course Designer(s)

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SoC Design for IoT

Course Code	VLS 485	Course Category	Professional Core (C)	L-T-P-C	3	0	0	3
Pre-Requisite Course(s)	Microprocessors and Microcontrollers	Co-Requisite Course(s)		Progressive Course(s)				
Course Offering Department	Electronics and Communication Engineering	Professional / Licensing Standards						

Course Objectives / Course Learning Rationales (CLRs)

Objective 1: Understand the basics of SoC Design.

Objective 2: Learn the techniques to choose a processor for SoC Implementation.

Objective 3: Learn different type of memory blocks used in SoC Design.

Objective 4: Understand the bus architecture and Custom SoC Design.

Objective 5: Learn the designing methods for customized SoC Design using hardware and software co-design.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course, the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Understand and explain the basics of SoC Design.	2	80%	70%
Outcome 2	Understand the techniques in choosing a best processor for SoC implementation.	3	80%	70%
Outcome 3	Understand the memory blocks used in SoC Design.	2	80%	70%
Outcome 4	Understand various bus architecture in designing Custom SoCs.	3	80%	70%
Outcome 5	Understand various terminologies using hardware and software co-design for designing customized SoC using suitable Processor.	2	80%	70%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)												
	Engineering Knowledge	Conduct Investigations of Complex Problems	Design and Development	Modern Tool Usage	Society and Multicultural Skills	Environment and Sustainability	Moral, and Ethical Awareness	Individual and Teamwork Skills	Communication Skills	Life Long Learning	PSO1	PSO2	PSO3
Outcome 1	3	2	2	1				1		1	1	1	1
Outcome 2	3	3	3	2				1		2	2	2	2
Outcome 3	3	2	2	1				1		1	2	2	2
Outcome 4	3	3	2	1				1		2	2	2	2
Outcome 5	3	2	2	2				1		2	2	2	2
Course Average	**3**	**2**	**2**	**1**				**1**		**2**	**2**	**2**	**2**

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit 1	**SYSTEM ARCHITECTURE: OVERVIEW**	**9**		
1	Components of the system, Processor architectures	2	1	1,3
2	Processor architectures, Memory and addressing – system level interconnection.	2	1	1,3,4
3	SoC design requirements and specifications, Design integration – design complexity.	2	1	1,3,4
4	Cycle time, die area and cost, Ideal and practical scaling.	1	1	1,3,4
5	Design integration – design complexity, Area-time-power tradeoff in processor design.	1	1	1,3,4
6	Configurability.	1	1	1,3,4
Unit 2	**PROCESSOR SELECTION FOR SOC**	**9**		
7	Overview – soft processors.	1	**2**	1,3,4
8	Processor core selection.	1	2	1,3,4
9	Basic concepts – instruction set, branches.	1	2	1,3,4
10	Interrupts and exceptions.	1	2	1,3,4
11	Basic elements in instruction handling.	1	2	1,3,4
12	Minimizing pipeline delays	1	2	1,3,4
13	Reducing the cost of branches – Robust processors	1	2	1,3,4
14	Vector processors, VLIW processors	1	2	1,3,4
15	Superscalar processors.	1	2	1,3,4
Unit 3	**MEMORY DESIGN**	**9**		
16	SoC external memory, SoC internal memory	1	3	3
17	Scratch pads and cache memory	1	3	3
18	Cache organization and write policies	1	3	2, 3, 4
19	Srategies for line replacement at miss time	1	3	2,3
20	Split I- and D-	1	3	3,4
21	Caches – multilevel caches	1	3	3
22	SoC memory systems	**1**	3	1,4
23	Board based memory systems	1	3	2
24	Simple processor/memory interaction.	1	3	2
Unit 4	**INTERCONNECT ARCHITECTURES ANDSOCCUSTOMIZATION**	9		2
25	Bus architectures – SoC standard buses.	1	4	2
26	AMBA, Core Connect.	1	4	2,3
27	Processor customization approaches.	**1**	4	2,3
28	Reconfigurable technologies.	1	4	2
29	Mapping designs onto reconfigurable devices.	1	4	2
30	FPGA based design.	1	4	2
31	Architecture of FPGA.	**1**	4	2
32	FPGA interconnect technology.	1	4	2,4
33	FPGA memory, Floor plan and routing	1	4	2,3,4

Unit 5		9		
34	Hardware software task partitioning – FPGA fabric Immersed Processors	1	5	1,2
35	Soft Processors and Hard Processors	1	5	2,3,4
36	Tool flow for Hardware/Software Co-design	1	5	2,3
37	Interfacing Processor with memory and peripherals	1	5	2,3
38	Types of On-chip interfaces – Wishbone interface	1	5	2,3
39	Avalon Switch Matrix.	1	5	2,3,4
40	OPB Bus Interface	1	5	2,3
41	Creating a Customized Microcontroller	1	5	1,4
42	FPGA-based Signal Interfacing and Conditioning.	1	5	2,3,4
	Total Contact hours	**45**		

Recommended Resources

1. Michael J. Flynn and Wayne Luk**,** "Computer System Design: System-on-Chip", John Wiley and sons,2011.
2. Rahul Dubey, "Introduction to Embedded System Design Using Field Programmable Gate Arrays", Springer Verlag London Ltd.,2009.
3. Sudeep Pasricha and Nikil Dutt, On-Chip Communication Architectures - System on Chip Interconnect, Elsevier, 2008.
4. Steve Furber, System-on-chip Architecture, Addison-Wesley, 2000.

Learning Assessment

Bloom's Level of Cognitive Task		**Continuous Learning Assessments (50%)**								**End Semester Exam (50%)**	
		CLA-1 (10%)		**Mid-1 (20%)**		**CLA-II (10%)**		**CLA-III (10%)**			
		Th	**Prac**	**Th**	**Prac**	**Th**	**Prac**	**Th**	**Prac**	**Th**	**Prac**
Level 1	Remember	40%		30%		40%		40%		50%	
	Understand										
Level 2	Apply	60%		70%		60%		60%		50%	
	Analyse										
Level 3	Evaluate										
	Create										
Total		100%		100%		100%		100%		100%	

Course Designers

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FPGA-based Embedded System Design

Course Code	VLS 486	**Course Category**	Technical Elective	**L-T-P-C**	2	0	1	3
Pre-Requisite Course(s)		**Co-Requisite Course(s)**		**Progressive Course(s)**				
Course Offering Department	ECE	**Professional / Licensing Standards**	*VIVADO*					

Course Objectives / Course Learning Rationales (CLRs)

Objective 1: To introduce the internal architecture of programmable logic with focus on FPGA.

Objective 2: To provide knowledge in FPGA design flow at the architectural and system design.
Objective 3: To impart a good background in block-based design using standard system level tools.

Course Outcomes / Course Learning Outcomes (CLOs)

	At the end of the course the learner will be able to	Bloom's Level	Expected Proficiency Percentage	Expected Attainment Percentage
Outcome 1	Ability to understand the structure of the fabric of programmable logic	2	80%	75%
Outcome 2	Implement ideas on Placement and Partitioning of Circuits	3	80%	75%
Outcome 3	Identify concepts and Algorithms of Floor planning and Routing	3	80%	75%
Outcome 4	Develop circuit level techniques and apply in logic Synthesis	3	80%	75%
Outcome 5	Working on High Level Synthesis of Circuits	4	80%	75%

Course Articulation Matrix (CLO) to Program Learning Outcomes (PLO)

CLOs	Program Learning Outcomes (PLO)														
	Engineering Knowledge	Problem Analysis	Design and Development	Analysis, Design and Research	Modern Tool and ICT Usage	Society and Multicultural Skills	Environment and Sustainability	Moral, and Ethical Awareness	Individual and Teamwork Skills	Communication Skills	Project Management and Finance	Self-Directed and Life Long Learning	PSO 1	PSO 2	PSO 3
Outcome 1	3	3	3	3	1		2	1				3	3	1	2
Outcome 2	3	3	3	3	2	1	2	1	3			2	3	2	2
Outcome 3	3	3	3	3	2		2	1	3			3	3	2	2
Outcome 4	3	3	3	3	2	1	2	1	3			2	3	2	2
Outcome 5	3	3	3	3	2	1	2	1	2			2	3	2	2
Course Average	**3**	**3**	**3**	**3**	**2**	**1**	**2**	**1**	**3**			**2**	**3**	**2**	**2**

Course Unitization Plan

Unit No.	Unit Name	Required Contact Hours	CLOs Addressed	References Used
Unit 1	**Programmable Logic Devices**	**10**		
	PROM - PAL - PLA - CPLD - Gate Arrays - MPGA	1	1	1
	FPGA - Programming Technologies - EPROM - EEPROM - FLASH - SRAM - FPGA Fabric	2	1	1

	Configurable Logic Block - LUT - Slice - Slicem	1	1	1
	Programmable Interconnects - Input Output Blocks - Keeper Circuit - Xilinx 7 Series Architecture.	2	1	1
	Introduction to Edge Zynq SoC FPGA Development Board. (Lab Experiment - 1)	2	1	4
	Controlling LED in Edge Zynq SoC FPGA Development Board. (Lab Experiment - 2)	2	1	4
Unit 2	**FPGA Design Flow and Abstraction Levels**	**10**		
	Verilog Design for Synthesis	1	2	1
	One Hot Encoding - Memory Blocks - Block Memory Generator (BRAM/BROM)	2	2	1
	Single Port Memory - Dual Port Memory	1	2	2
	FIFO - Distributed RAM - Synthesis Pitfalls - Latch Inference	2	2	2
	Designing Combinational Logic circuits Edge Zynq SoC FPGA Development Board. (Lab Experiment - 3)	2	2	5
	Designing Sequential Logic circuits Edge Zynq SoC FPGA Development Board. (Lab Experiment - 4)	2	2	5
Unit 3	**Static Timing Analysis**	**14**		
	Speed Performance - Timing Constraints	2	3	2
	Clock Management - Clock Buffers.	3	3	2
	Clock Tree Routing	3	3	2
	Control relay using switch on the Edge Zynq Board. (Lab Experiment - 5)	2	3	5
	Produce sound at piezo Buzzer at regular interval on Edge Zynq Board. (Lab Experiment - 6)	2	3	5
	LDR Interface using ADC. (Lab Experiment - 7)	2	3	5
Unit 4	**Introduction to SoC Design**	**10**		
	Hard Macros - Multipliers - DSP Block	2	4	3

	Hard Core Processors - Interface Circuits	2	4	3
	Configuration Chain - JTAG Interface - Zynq7000 Architecture	2	4	3
	2x16 Liquid Crystal Display Interface. (Lab Experiment - 8)	2	4	4
	4-bit BCD to Seven Segment Display. (Lab Experiment - 9)	2	4	4
Unit 5	**Timing Simulation and Programming**	**10**		
	Timing Simulation using Modelsim/Icarusverilog,	2	5	3
	Programming using JTAG, System Level testing and debugging	1	5	3
	Debugging techniques	1	5	3
	Debugging using chip scope and Logic analyzers, Protocols on FPGA	2	5	3
	Seven Segment Display Counter. (Lab Experiment - 10)	2	5	3
	Displays 128x160 pixel image on the SPI TFT Display interfaced to Edge board. (Lab Experiment - 11)	2	5	4
	Project			

Recommended Resources

. 1. Amano, Hideharu, Principles and Structures of FPGAs, First Edition, Springer, 2018.
2. Readler, Blaine C., Verilog by example: a concise introduction for FPGA design, Full Arc Press, 2011.
3. ZainalabedinNavabi, Embedded Core Design with FPGAs, First Edition, McGraw Hill, 2008.
4. Xilinx Inc, Vivado Design Suite User Guide, 2021.

Learning Assessment

Bloom's Level of Cognitive Task		**Continuous Learning Assessments (50%)**								**End Semester Exam (50%)**	
		CLA-1 (10%)		**Mid-1 (15%)**		**CLA-2 (10%)**		**CLA3 (15%)**			
		Th	**Prac**	Th	Prac	**Th**	**Prac**	**Th**	**Prac**	**Th**	**Prac**
Level 1	Remember	60%	30%	50%	40%	60%	30%	50%	40%	50%	50%
	Understand										
Level 2	Apply	40%	50%	50%	50%	40%	60%	50%	50%	40%	40%
	Analyze										
	Evaluate		20%		10%		10%		10%	10%	10%

Level 3	Create										
Total		**100%**	**100%**	**100%**	**100%**	**100%**	**100%**	**100%**	**100%**	**100%**	**100%**

Course Designers

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